DKT217/3

COMPUTER SYSTEM
[SISTEM KOMPUTER]

CONTINUOUS ASSESSMENT

DATE   WEDNESDAY, 15th APRIL 2020
TIME   10.00pm ~ 11.00pm (1 hour)

INSTRUCTIONS
- Use your own paper to answer.
- Answers must be handwritten.
- Your name, matric and page number MUST be written on every answer page.
- Scan and save in PDF format only.
- Upload/Email the PDF file BEFORE 10.55pm
- For Quartus II projects, make sure all your projects are in a folder with the foldername YOUR NAME and MATRIC as proof of work.

QUESTION 1

(a)   Figure 1 below is a diagram of a bit register. Using the VHDL code, complete the programme for the bit register as in Figure 2.
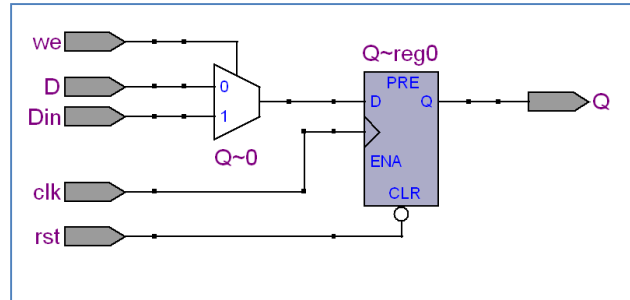

Figure 1: Schematic of a bit register

```
LIBRARY IEEE;
use IEEE.STD_LOGIC_1164.ALL;


ENTITY bit_reg IS
PORT (      we, D, Din, clk, rst    : IN    STD_LOGIC;
            Q                        : OUT  STD_LOGIC  );
END bit_reg;


ARCHITECTURE beh OF bit_reg IS
BEGIN
        PROCESS (_____)
        BEGIN
              IF _____ THEN
                   Q <= '0';

              ELSIF _____ THEN

                    IF _____ THEN

                          Q <= Din;
                    ELSE
                          Q <= D;
                    END IF
              END IF;
        END PROCESS;
END beh;
```

Figure 2: VHDL programme of a bit register

(b) Figure 3 below is a schematic diagram of the bit register in Question 1(a) connected together to become a 4 bit shift-right register. An incomplete VHDL program is shown below. Complete the program to satsify Figure 3.
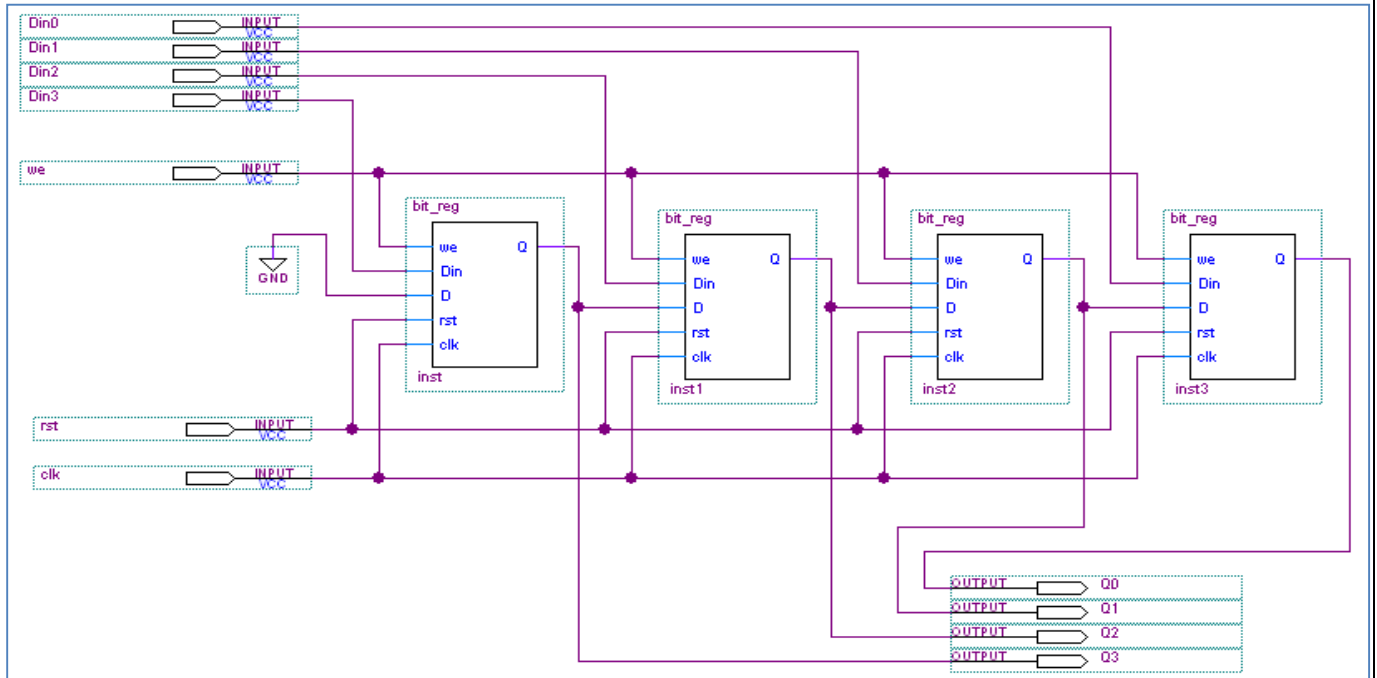

Figure 3: Schematic diagram of a 4-bit Shift Right Register with synchronous parallel input

```
LIBRARY IEEE;
use IEEE.STD_LOGIC_1164.ALL;

ENTITY sr_reg4 IS
PORT (      Din            : in     std_logic_vector(3 downto 0);
            rst,clk,we     : in     std_logic;
            Q              : out    std_logic_vector(3 downto 0) );
END sr_reg4;

ARCHITECTURE beh OF sr_reg4 IS

COMPONENT bit_reg
PORT (      we, Din, D, rst, clk    : in     std_logic;
            Q                       : out    std_logic );
END component;
:
: - complete this program for Figure 3.
```
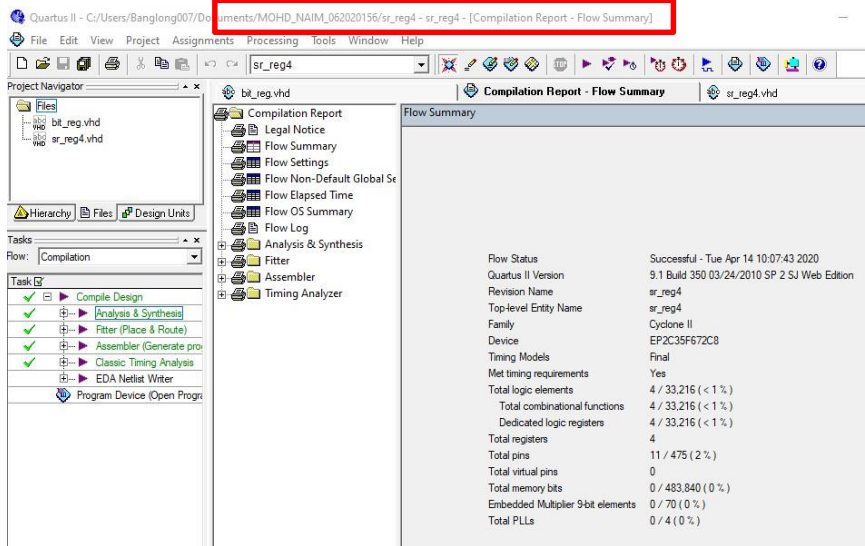
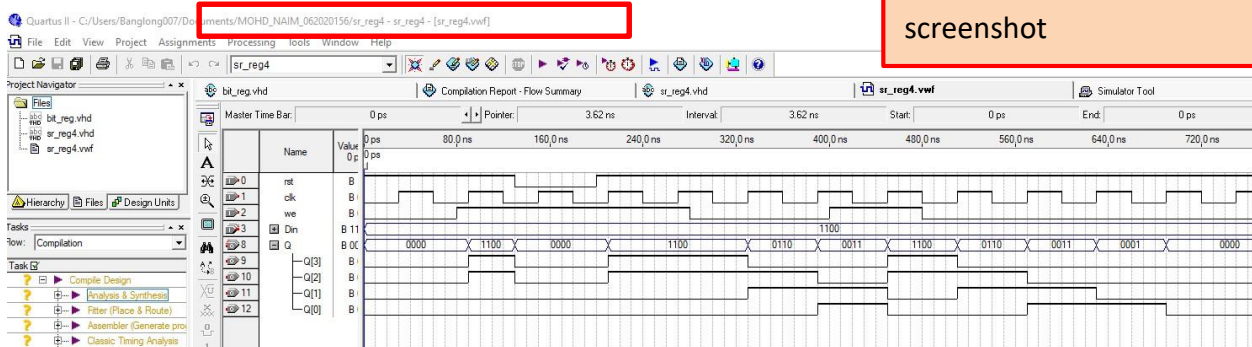(c)   Attach the following figures to prove your project is successful.

1. Successful compilation report that shows your Project Folder (Name & Matric) and Project Name
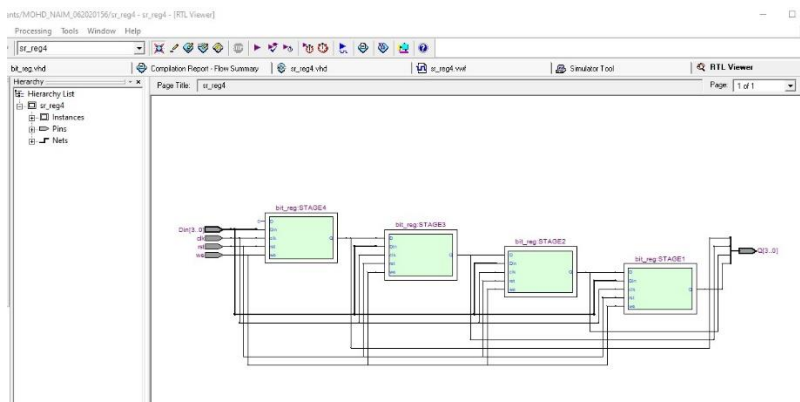

All screenshots must clearly show your project folder and active projects (in the red boxes).

2. Waveform

Waveform setting :
End Time : 800ns
Grid Size : 10ns
Waveform and IO as shown in screenshot

3. RTL (optional)

QUESTION 2

The following VHDL program for an ALU has several errors detected in them when compiled using the Altera Quartus II software. Create a 3-column table (as shown below) to
1. **Identify the lines containing the error,**
2. **Brief explanation about the error**
3. **Proposed corrected line**

Line
```
1     library ieee;
2     use ieee.std_logic_1164_all;
3     use ieee.std_logic_arith_all;
4     use ieee.std_logic_unsigned_all;
5
6     entity test_alu4 is
7     port (   inA, inB, outC          : in     std_logic_vector(3 downto 0);
8              Sel                      : in     std_logic_vector(1 downto 0);
9              Carry, Bigger            : out    std_logic);
10    end test_alu4;
11
12    architecture labtest of test_alu4 is
13            temp : std_logic_vector(4 downto 0);
14    begin
15            process (inA, inB, sel, temp)
16                    Bigger <= "0";
17                    Case sel is
18                    When "00" =>
19                            temp <= ("0" & inA) + ("0" & inB);
20                            outC <= temp(4 downto 1);
21                            Carry <= temp(0);
22                    When "01" =>
23                            If inA => inB then
24                                    outC <= inA – inB;
25                                    Bigger <= "0";
26                            Else
27                                    outC <= inB – inA;
28                                    Bigger <= "1";
29                    When "10" =>
30                            outC <= inA and inB;
31                    When "others" =>
32                            outC <= inA or inB;
33                    end case;
34            end process
35    end test_alu4;
```

Line No.	Brief explanation on error	Propose correction

* * * * * * * * * G O O D * * * * * * * * * * * * * * L U C K * * * * * * * * * * * * *