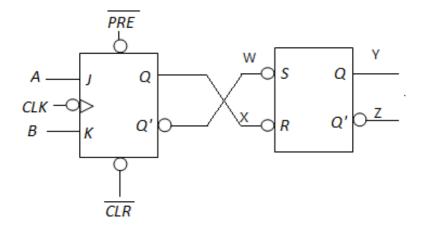
PAPER 1 (CO1, C4)

This part has TWO (2) questions. Answer ALL questions. (30 marks).

Question 1

Figure 1 shows a combination of flip-flops and latch. Draw the output waveform of signals *W*, *X*, *Y* and *Z* in **Appendix I**. Assume that all the output values are initially at 0.

(15 Marks)





Question 2

Sketch the logic diagram of 4-bit SIPO shift register using D flip-flops. Then, develop the timing diagram of 4-bit SIPO shift register using D flip flop. Let the input data $Q_3Q_2Q_1Q_0=0111$. Complete the outputs for Q_3 , Q_2 , Q_1 and Q_0 for four(4) clock cycles. Assume that the register initially contains all 1's.

Complete your answer in Appendix 2.

(15 marks)

Appendix 1

Question 1

Angka Giliran:_____

Nama:

ID:_____

CLK										
CLR										
PRE										
Α						 				
В								 		
w										
x										
Y										
Z										

Appendix 2

Question 2

Angka Giliran:_____

Nama:

ID:_____

4-bit SIPO shift register using D flip-flops:

The complete output:

CLK					
Data Input					
Qo					
Q ₁					
Q ₂					
Q ₃					