
UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Pertama
Sidang Akademik 2020/2021

TEST 1

DKT 212 – Digital System II
[Sistem Digit II]

Duration: 2 hour

Please make sure that this question paper has **FOUR (4)** printed pages including this front page before you start the examination.

This question paper has **THREE** questions. Answer **all** questions.

NAME :

MATRIX ID:

PROGRAM :

SCHOOL :

GROUP :

Q 1 / 10	Q 2 / 10	Q3 / 20	TOTAL MARKS / 40

QUESTION 1 (10 Marks)

- a) State **TWO** differences between Latch and Flip-flop. (2 Marks)
- b) List two types of classes Flip-flop. (2 Marks)
- c) Explain briefly the operation of “positive edge-triggered” J-K Flip-flop. (2 Marks)
- d) For a positive edge-triggered J-K flip-flop with the inputs as shown in Figure 1 below, determine either “LOW” or “HIGH” for the outputs (I,II,III,IV,V,VI,VII,VIII) relative to the clock. Assume that Q is RESET. (4 Marks)

(Example answer : I is HIGH)

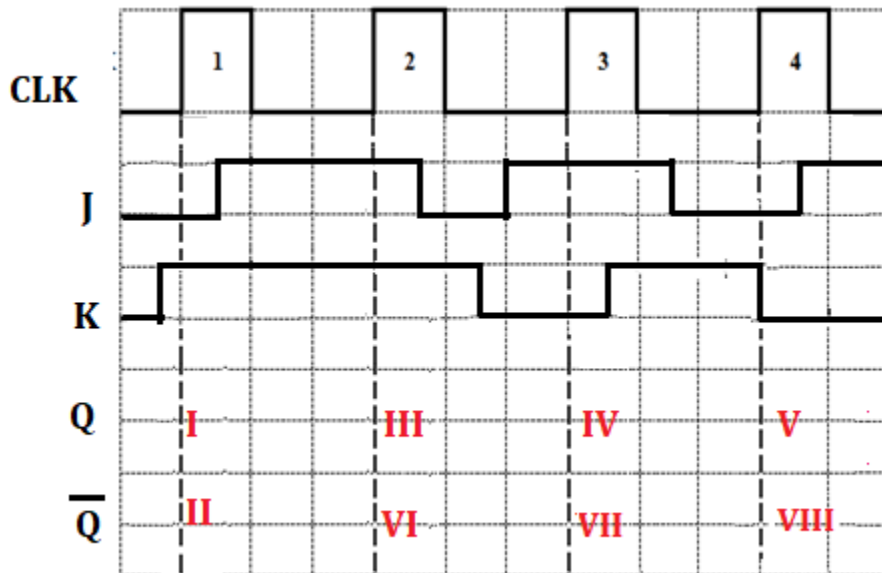


Figure 1

QUESTION 2 (10 Marks)

a) State **TWO** basic operations of register. (2 Marks)

b) By using four bit data, illustrate the basic movement for the following type of shift register operation. (4 Marks)

- i) Serial in/serial out
- ii) Serial in/Parallel out
- iii) Parallel in/serial out
- iv) Parallel in/parallel out

c) The following Figure 2(a), Serial in/serial out which accept the data serially. A serial input is given below. Show the entry of the given input and obtain the outputs that will produce as Serial out into the table in Figure 2(b). (4 Marks)

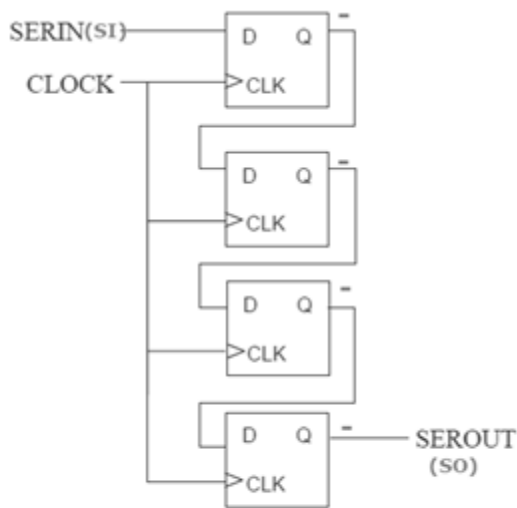


Figure 2(a)

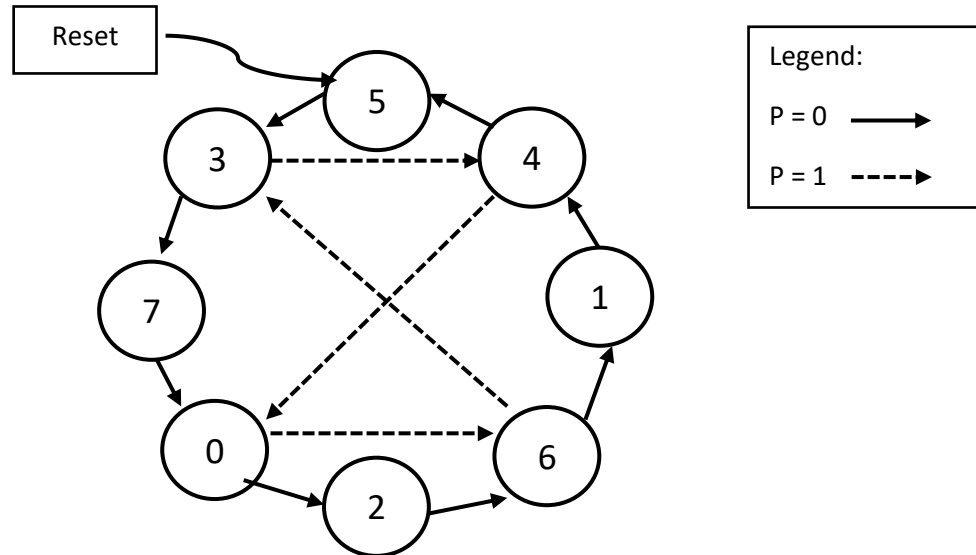
Serial input : 1010110010

SI	1									
SO	-									

Figure 2(b)

QUESTION 3 (20 Marks)

Figure 3 below shows a certain bi-directional synchronous counting sequence where the variable P is the sequence direction controller.



- Construct the Present State – Next State table for the counting sequence above. (2 marks)
- Derive the JK Flip-flop state transition diagram and obtain the respective JK input values for the constructed Present State – Next State table. (6 marks)
- Use the Karnaugh mapping technique and obtain the respective JK input simplified Boolean equations. (6 marks)
- Draw the JK Flip-flop counter circuit complete with the appropriate inputs and outputs. (6 marks)