UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Pertama
Sidang Akademik 2016/2017

Oktober 2016

DMT 231 – Analogue Electronics
[Elektronik Analog]

Masa : 3 jam

Please make sure that this question paper has **THIRTEEN (13)** printed pages including this front page before you start the examination.
*[Sila pastikan kertas soalan ini mengandungi **TIGA BELAS (13)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This question paper has **SIX (6)** questions. Answer any **FIVE (5)** question. Each question contribute 20 marks.
*[Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab mana-mana **LIMA (5)** soalan. Setiap soalan menyumbang 20 markah.]*

List of equation is given in **Appendix.**
*[Senarai persamaan diberikan pada **Lampiran.**]*

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Question 1
[Soalan 1]

(a) Sketch the symbols for Bipolar Junction Transistor (BJT).
[Lakarkan simbol-simbol bagi Transistor Simpangan Dwipolar (BJT).]

(4 Marks/ *Markah*)

(b) State **THREE (3)** basic types of BJT amplifiers.
*[Nyatakan **TIGA (3)** jenis penguat BJT asas.]*

(3 Marks/ *Markah*)

(c) **Figure 1** shown amplifier circuit with $\beta = 100$ and $V_{EB\,(ON)} = 0.7$ V. Determine;
*[**Rajah 1** menunjukkan litar penguat dengan $\beta = 100$ dan $V_{EB\,(ON)} = 0.7$ V. Tentukan;]*

(i) type of amplifier configuration for this amplifier circuit.
[jenis konfigurasi penguat untuk litar penguat ini.]

(2 Marks/ *Markah*)

(ii) quiescent base current, I_{BQ}.
[arus tapak sepi, I_{BQ}.]

(3 Marks/ *Markah*)

(iii) quiescent base current, I_{CQ}.
[arus pemungut sepi, I_{CQ}]

(3 Marks/ *Markah*)

(iv) quiescent emitter current, I_{EQ}.
[arus pemancar sepi, I_{EQ}]

(2 Marks/ *Markah*)

(v) quiescent emitter-collector voltage, V_{ECQ}.
[voltan pemancar- pemungut sepi , V_{ECQ}]

(3 Marks/ *Markah*)

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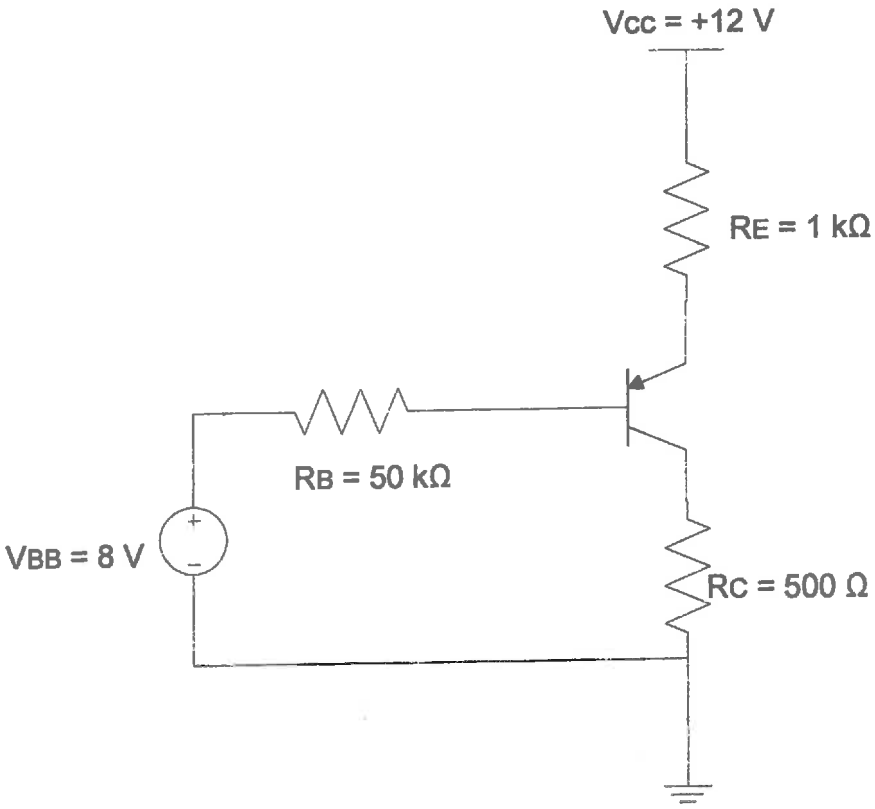

Figure 1
[Rajah 1]

Question 2
[Soalan 2]

(a) State **TWO (2)** rules of AC analysis for small signal BJT circuits.
*[Nyatakan **DUA (2)** peraturan-peraturan bagi analisis AC untuk isyarat kecil litar BJT.]*
(2 Marks/ *Markah*)

(b) Circuit in **Figure 2** shows a common emitter amplifier circuit with $\beta = 100$, $V_{BE(on)} = 0.7$ V, $V_T = 26$ mV and $V_A = 100$. Based on **Figure 2**, determine;
*[Litar dalam **Rajah 2** menunjukkan satu litar penguat pemancar sepunya dengan $\beta = 100$, $V_{BE(on)} = 0.7$ V, $V_T = 26$mV dan $V_A = 100$. Berdasarkan pada **Rajah 2**, tentukan;]*

(i) Thevenin resistor, R_{TH}.
[perintang Thevenin, R_{TH}.]
(2 Marks/ *Markah*)

(ii) Thevenin voltage, V_{TH}
[voltan Thevenin, V_{TH}.]
(2 Marks/ *Markah*)

(iii) base current, I_{BQ}.
[arus tapak , I_{BQ}.]
(2 Marks/ *Markah*)

(iv) collector current, I_{CQ} and collector-emitter voltage, V_{CE}.
[arus pemungut , I_{CQ} dan voltan pemancar-pemungut , V_{CE}.]
(4 Marks/ *Markah*)

(v) sketch small signal equivalent circuit.
[lakarkan litar setara isyarat kecil]
(4 Marks/ *Markah*)

(vi) diffusion resistance, r_π.
[rintangan resapan, r_π.]
(1 Mark/ *Markah*)

(vii) output resistance, r_o.
[rintangan keluaran , r_o.]
(1 Mark/ *Markah*)

(viii) small signal voltage gain, A_v
[isyarat kecil gandaan voltan, A_v]
(2 Marks/ *Markah*)

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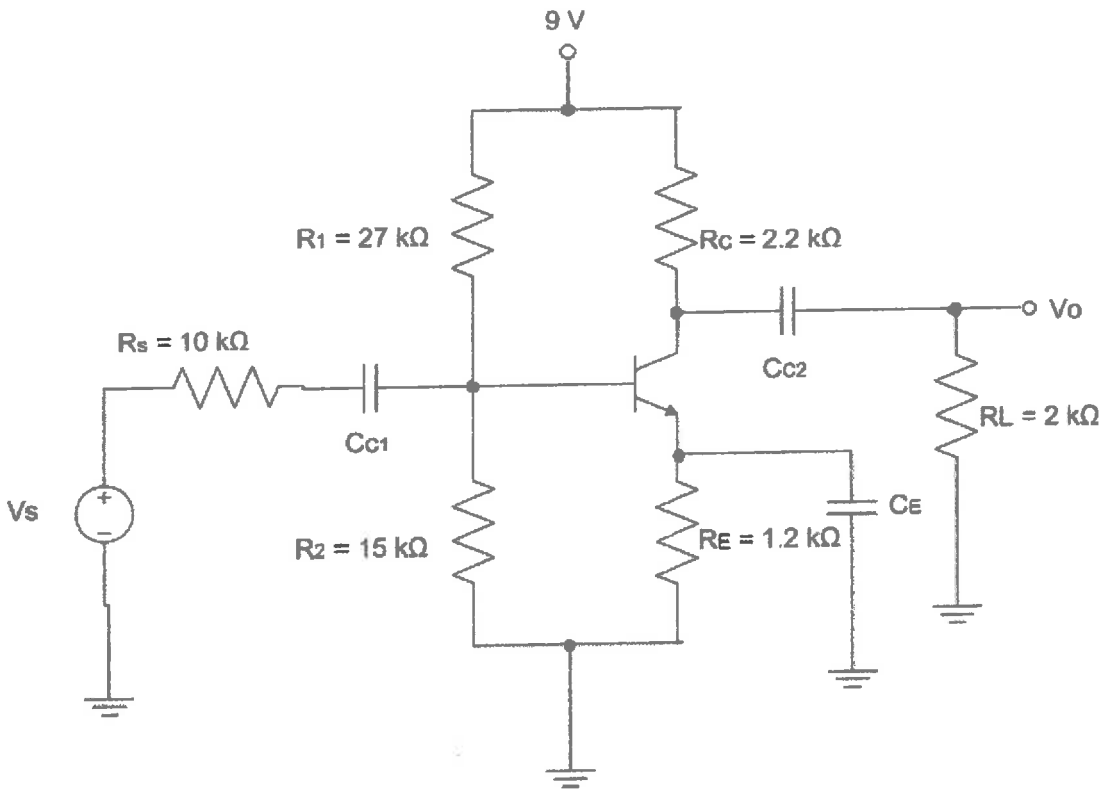

Figure 2
[*Rajah 2*]

Question 3
[Soalan 3]

(a) State **TWO (2)** advantages of FET device.
*[Nyatakan **DUA (2)** kelebihan-kelebihan peranti FET.]*

(2 Marks / *Markah*)

(b) Sketch the symbol for both channels JFET.
[Lakarkan simbol bagi kedua-dua saluran JFET.]

(2 Marks / *Markah*)

(c) **Figure 3** below show the transistor parameters are I_{DSS} = 2mA, V_P = -2V and $\lambda = 0$. Based on **Figure 3;**
[Rajah 3** di bawah menunjukkan parameter-parameter transistor adalah IDSS = 2mA, VP = -2V dan $\lambda = 0$. Berpandukan pada **Rajah 3;]

(i) State the circuit configuration.
[Nyatakan tatarajah litar.]

(1 Mark / *Markah)*

(ii) Sketch the small- signal equivalent circuit for the circuit.
[Lakarkan litar setara isyarat kecil untuk litar.]

(5 Marks / *Markah*)

(iii) Calculate gate-source voltage, V_{GS}.
[Kirakan voltan pintu sumber, V_{GS}.]

(6 Marks / *Markah*)

(iv) Calculate transconductance, g_m.
[Kirakan transkonduksian, g_m.]

(2 Marks / *Markah*)

(v) Calculate small-signal voltage gain $A_v = v_o / v_i$.
[Kirakan gandaan voltan isyarat kecil, $A_v = v_o / v_i$.]

(2 Marks / *Markah*)

....7/-

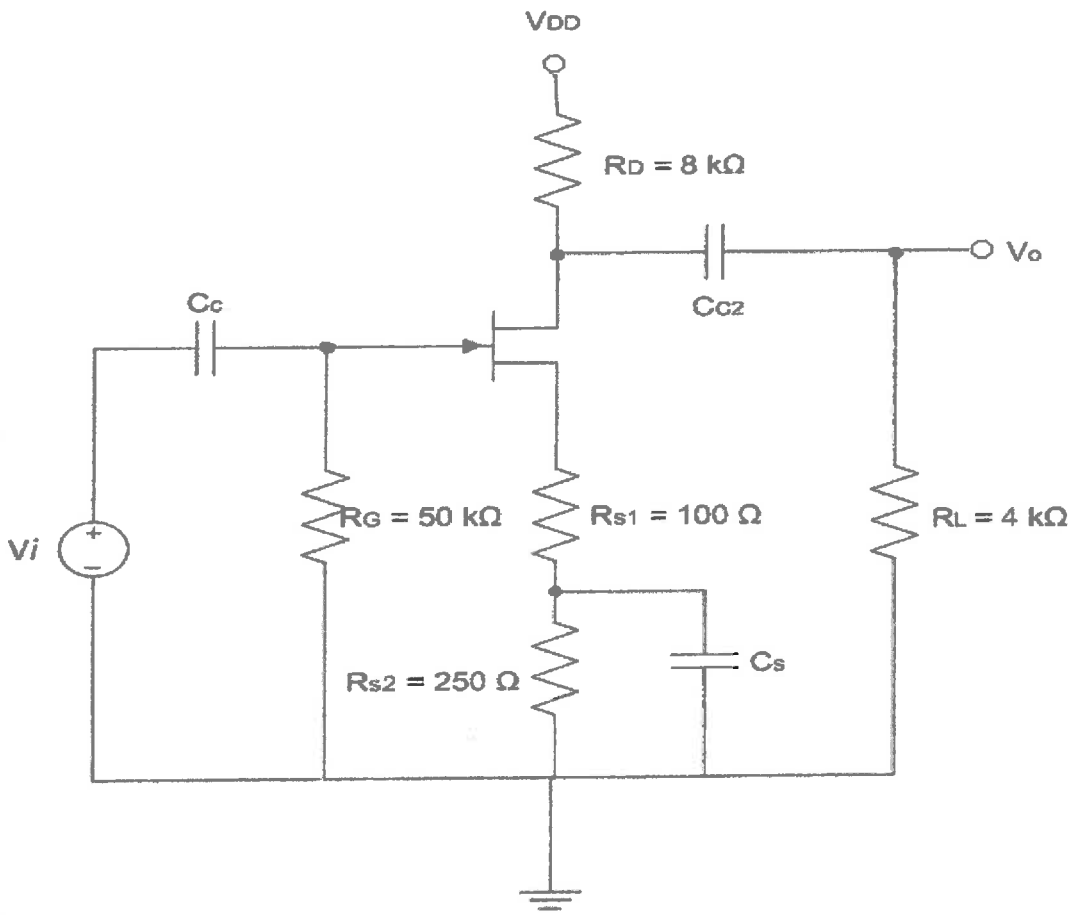

Figure 3
[Rajah 3]

Question 4
[Soalan 4]

Figure 4 shows a cascaded configuration as part of a multistage amplifier. The circuit elements transistor Q_1 and Q_2 are $\beta_1 = \beta_2 = 125$, $V_{BE(ON)} = 0.7V$ and $r_o = \infty$. Based on **Figure 4**, analyse;
***[Rajah 4** menunjukkan konfigurasi terlatar sebagai sebahagian daripada penguat berbilang tahap. Elemen-elemen transistor Q_1 dan Q_2 adalah $\beta 1 = \beta 2 = 125$, $V_{BE(ON)} = 0.7V$ dan $r_o = \infty$. Berpandukan **Rajah 4**, analisakan;]*

(i) Thevenin resistor and voltage, R_{BB} and V_{BB}.
[voltan dan rintangan Thevenin , R_{BB} dan V_{BB}.]
(2 Marks/ *Markah*)

(ii) transistor Q_1 quiescent current, I_{BQ1}, I_{CQ1} and I_{EQ1}.
[arus sepi transistor Q_1 , I_{BQ1}, I_{CQ1} dan I_{EQ1}.]
(3 Marks/ *Markah*)

(iii) transistor Q_2 quiescent current, I_{BQ2}, I_{CQ2} and I_{EQ2}.
[arus sepi transistor Q_2 , I_{BQ2}, I_{CQ2} dan I_{EQ2}.]
(3 Marks/ *Markah*)

(iv) transistor Q_1 voltage, V_{C1} and V_{E1}.
[voltan transistor Q_1 , V_{C1} dan V_{E1}.]
(2 Marks/ *Markah*)

(v) transistor Q_2 voltage, V_{C2} and V_{E2}.
[voltan transistor Q_2 , V_{C2} dan V_{E2}.]
(2 Marks/ *Markah*)

(vi) transistor Q_1 and Q_2 quiescent voltage, V_{CEQ1} and V_{CEQ2}.
[voltan sepi transistor Q_1 dan Q_2, V_{CEQ1} dan V_{CEQ2}.]
(2 Marks/ *Markah*)

(b) Sketch small signal equivalent circuit for circuit configuration shown in **Figure 4.**
*[Lakarkan litar setara isyarat kecil bagi konfigurasi litar yang ditunjukkan dalam **Rajah 4.**]*
(6 Marks/ *Markah*)

....9/-

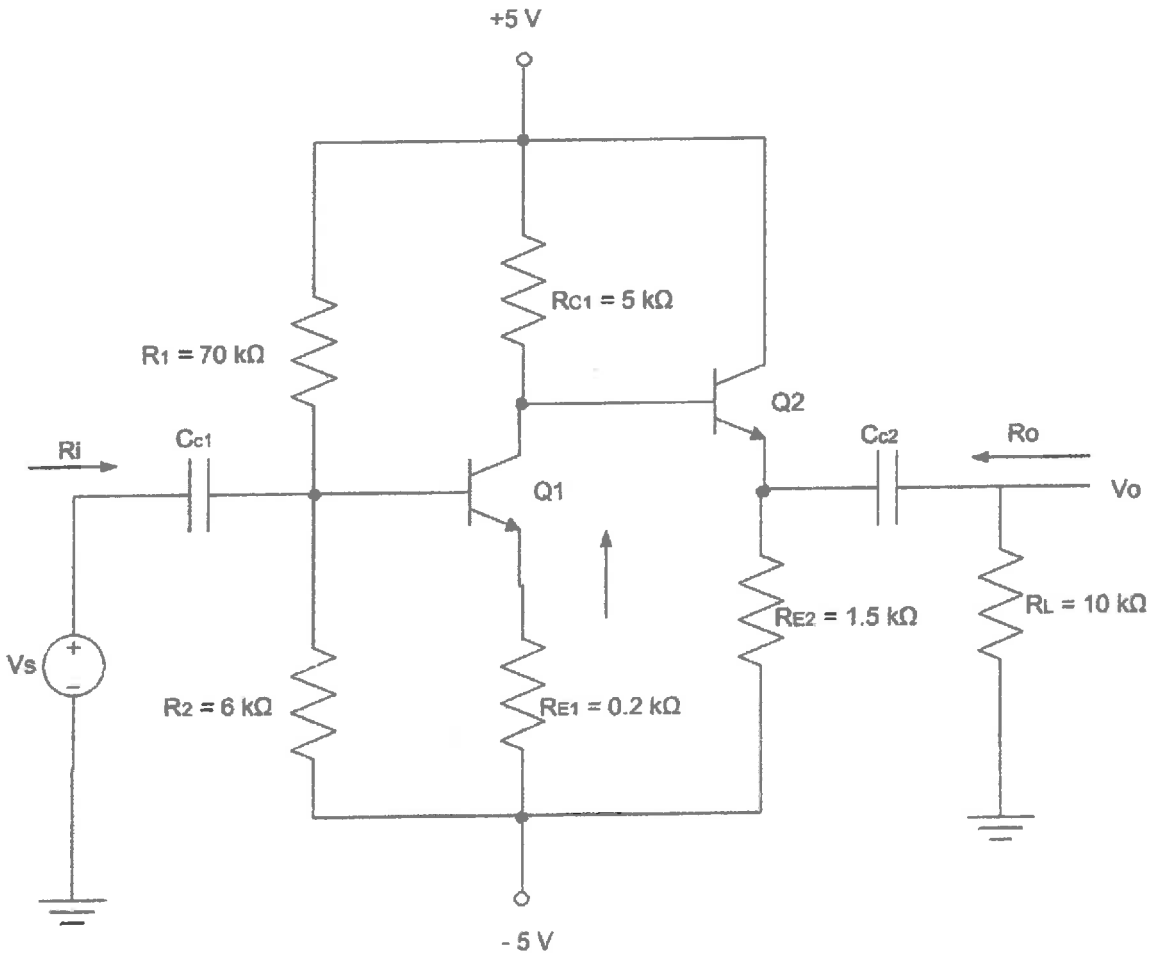

Figure 4
[Rajah 4]

Question 5
[Soalan 5]

(a) Power amplifiers are generally classified according to the percent of time the output transistors are conducting.
[Penguat-penguat kuasa dikelaskan secara umum mengikut peratus masa masukan pengaliran transistor.]

(i) List **FOUR (4)** types classification of power amplifiers.
*[Senaraikan **EMPAT (4)** kelas penguat-penguat kuasa.]*

(4 Marks/ *Markah*)

(ii) From a(i) sketch and label all class of power amplifiers.
[Daripada a(i) lukis dan label semua kelas penguat-penguat kuasa.]

(6 Marks/ *Markah*)

(b) **Figure 5** shows a power amplifier stage using enhancement-mode MOSFET and the transistors are matched. Given V_{DD} = 10 V, R_L = 20 Ω, K = 0.20 A/V^2, |VT| = 1 V and I_{DQ} is to be 20 percent of the load current when *Vo = 5 V.*
*[**Rajah 5** menunjukkan peringkat penguat kuasa menggunakan MOSFET mod peneguhan dan transistor dipadankan. Diberi V_{DD} = 10 V, R_L = 20 Ω, K = 0.20 A/V^2, |VT| = 1 V dan I_{DQ} adalah menjadi 20 peratus daripada arus beban semasa apabila Vo = 5 V.]*

(i) State the class of power amplifier configuration in **Figure 5**.
*[Nyatakan kelas bagi konfigurasi penguat kuasa dalam **Rajah 5**.]*

(2 Marks / *Markah*)

(ii) Determine the quiescent drain current, I_{DQ}.
[Tentukan arus longkang sepi, I_{DQ}.]

(2 Marks / *Markah*)

(iii) Calculate the gate-to-source voltage, V_{GSn} of M_n transistor.
[Kira voltan pintu sumber, V_{GS} transistor M_n.]

(2 Marks / *Markah*)

(iv) Calculate the source-to-gate voltage, V_{SGp} of M_p transistor.
[Kira voltan sumber pintu, V_{GS} transistor M_p.]

(2 Marks / *Markah*)

(v) Determine the input voltage of MOSFET, V_I.
[Tentukan voltan masukan MOSFET, V_I.]

(2 Marks / *Markah*)

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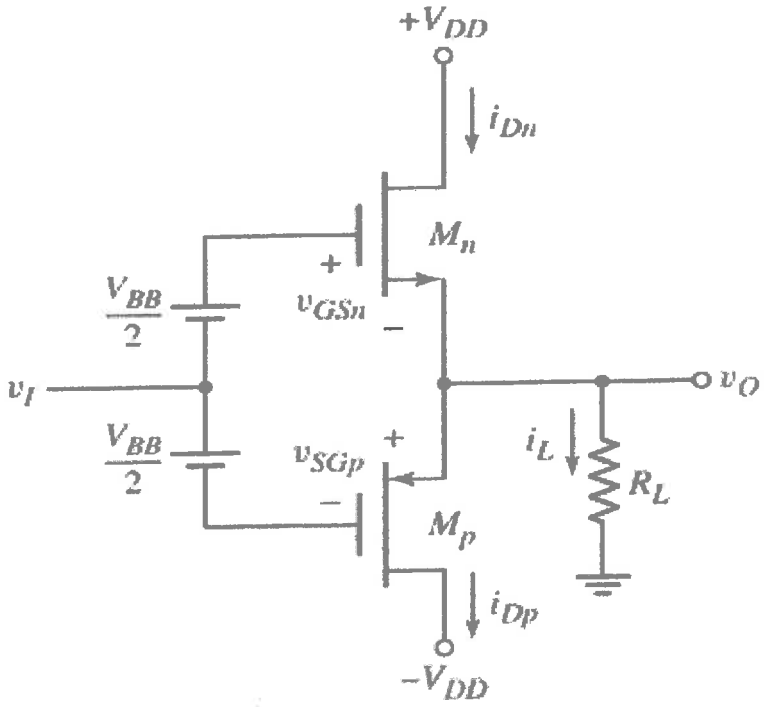

Figure 5
[Rajah5]

Question 6
[Soalan 6]

(a) State **THREE (3)** types of MOSFET amplifier.
*[Nyatakan **TIGA (3)** jenis penguat MOSFET.]*

(3 Marks / *Markah*)

(b) **Figure 6** below show the common-source amplifier with source resistor. Given $V_{TN} = 2$ V, $K = 1$ mA/V^2 and $\lambda = 0$. Determine;
***[Rajah 6** di bawah menunjukkan penguat biasa-sumber dengan sumber perintang. Diberi $V_{TN} = 2$ V, $K = 1$ mA/V^2 dan $\lambda = 0$. Tentukan;]*

(i) the equivalent dc analysis circuit.
[litar setara dc analisis.]

(4 Marks / *Markah*)

(ii) Q-point values for I_{DQ} *and* V_{DSQ}.
[nilai-nilai titik-Q bagi I_{DQ} dan V_{DSQ}.]

(4 Marks / *Markah*)

(iii) transconductance, g_m
[transkonduksian, gm.]

(2 Marks / *Markah*)

(iv) output voltage, *Vo*.
[voltan keluaran, Vo.]

(2 Marks / *Markah*)

(v) Sketch small signal equivalent circuit for circuit configuration shown in **Figure 6.**
*[Lakarkan litar setara isyarat kecil untuk litar konfigurasi yang ditunjukkan dalam **Rajah 6.**]*

(5 Marks / *Markah*)

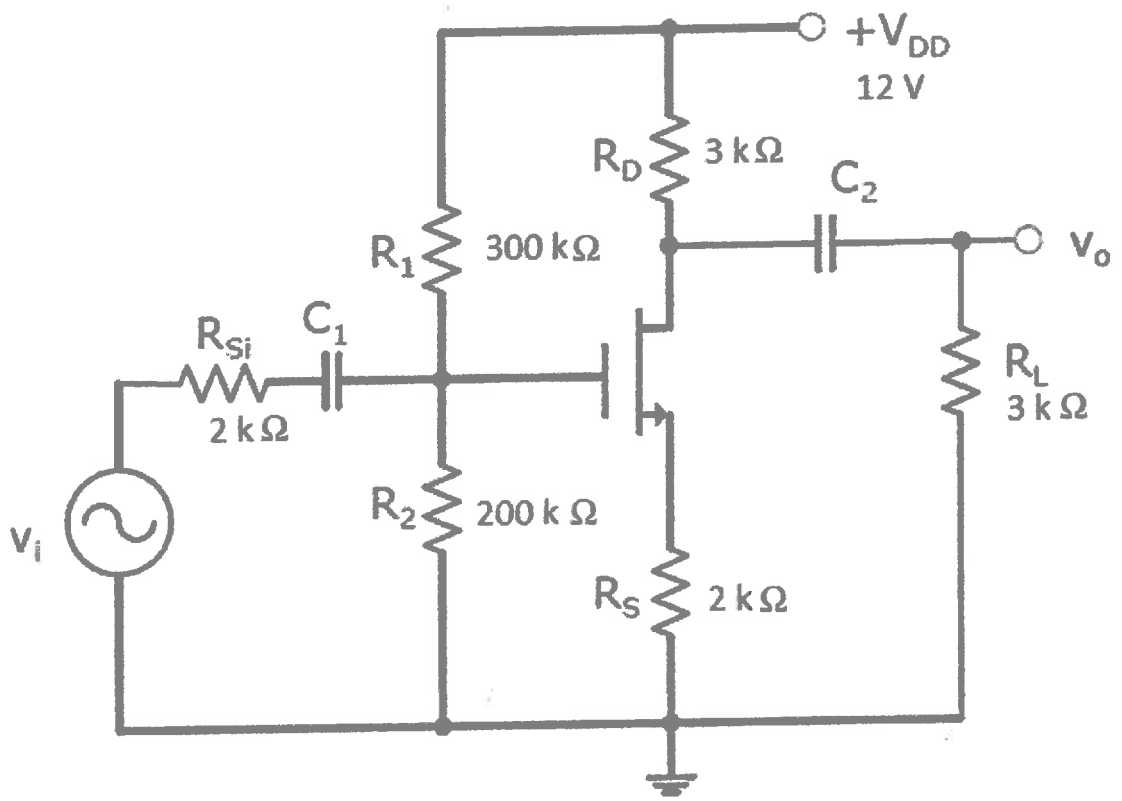

Figure 6
[Rajah 6]

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Appendix

[Lampiran]

1. $g_m = \frac{I_{CQ}}{V_T}$

2. $g_m = 2K_n(V_{GS} - V_{TN})$

3. $g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$

4. $A_v = -g_m R_C\left(\frac{r_\pi}{r_\pi + R_D}\right)$

5. $A_v = -g_m\left(\frac{R_1 \parallel R_2 \parallel r_\pi}{(R_1 \parallel R_2 \parallel r_\pi) + R_S}\right)(R_C \parallel r_o)$

6. $A_v = -\frac{\beta R_C}{r_\pi + (1+\beta)R_E}\left(\frac{R_i}{R_i + R_S}\right)$

7. $A_v = \frac{(1+\beta)(r_o \parallel R_E)}{r_\pi + (1+\beta)(r_o \parallel R_E)}\left(\frac{R_i}{R_i + R_S}\right)$

8. $A_v = g_m\left(\frac{R_C \parallel R_L}{R_S}\right)\left(\frac{r_\pi}{1+\beta} \parallel R_E \parallel R_S\right)$

9. $A_v = -g_m(r_o \parallel R_D)$

10. $A_v = \frac{-g_m(r_o \parallel R_D \parallel R_L)}{1 + g_m R_S}$

11. $A_v = -g_m(r_o \parallel R_D \parallel R_L)\left(\frac{R_i}{R_i + R_{Si}}\right)$

12. $A_v = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}\left(\frac{R_i}{R_i + R_{Si}}\right)$

13. $A_v = \frac{g_m(r_o \parallel R_D \parallel R_L)}{1 + g_m R_{Si}}$

14. $A_v = -g_m(r_o \parallel R_D \parallel R_L)$

15. $A_v = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}$

16. $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

17. $I_D = K_N(V_{GS} - V_{TN})^2$

18. $V_{DS(sat)} = V_{GS} - V_{TN}$