UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Pertama
Sidang Akademik 2014/2015

14 Oktober 2014

DMT 231 – Analogue Electronics
[Elektronik Analog]

Masa : 3 jam

Please make sure that this question paper has **FIFTEEN (15)** printed pages including this front page before you start the examination.
*[Sila pastikan kertas soalan ini mengandungi **LIMA BELAS (15)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This question paper has **SIX (6)** questions in **TWO (2) Sections.** Answer **ALL** questions in **Section A** and **any ONE (1)** question in **Section B.**
*[Kertas soalan ini mengandungi **ENAM (6)** soalan dalam **DUA (2) Bahagian.** Jawab **SEMUA** soalan dalam **Bahagian A** dan **mana-mana SATU (1)** soalan dalam **Bahagian B.**]*

List of equation is given in **Appendix A.**
*[Senarai persamaan diberikan pada **Lampiran A.**]*

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Section A
[Bahagian A]

Question 1
[Soalan 1]

(a) Sketch the symbols for bipolar junction transistor (BJT).
[*Lakarkan simbol bagi transistor simpangan dwipolar (BJT).*]

(2 Marks/ *Markah*)

(b) Sketch and label the IV characteristics curve for BJT.
[*Lakarkan dan labelkan lengkungan sifat IV bagi BJT.*]

(3 Marks/ *Markah*)

(c) State **THREE (3)** basic types of BJT amplifiers.
[*Nyatakan **TIGA (3)** jenis penguat BJT asas.*]

(3 Marks/ *Markah*)

(d) State **TWO (2)** rules of AC analysis for small signal BJT circuits.
*[Nyatakan **DUA (2)** peraturan bagi analisis AC untuk isyarat kecil litar BJT.]*

(2 Marks/ *Markah*)

(e) The common emitter circuit elements shown in **Figure 1** are $V_{CC} = 12V$, $V_{BB} = 8V$, $R_C = 0.4k\Omega$, $R_E = 1.2k\Omega$, $R_B = 30k\Omega$, $\beta = 75$ *and* $V_{BE\,(ON)} = 0.7\ V$.
*[Elemen litar penguat pemancar sepunya yang ditunjukkan di **Rajah 1** adalah* $V_{CC} = 12V$, $V_{BB} = 8V$, $R_C = 0.4k\Omega$, $R_E = 1.2k\Omega$, $R_B = 30k\Omega$, $\beta = 75$ *and* $V_{BE\,(ON)} = 0.7\ V$.*]*

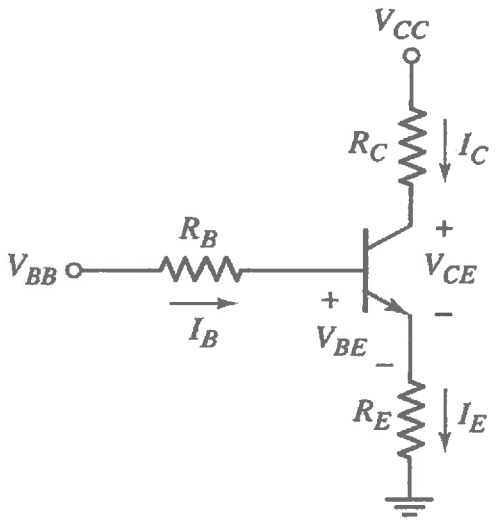

Figure 1
[*Rajah 1*]

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Determine;
[Tentukan;]

i) quiescent base current, I_{BQ}.
[arus tapak sepi, I_{BQ}]

(2 Marks/ *Markah*)

ii) quiescent collector current, I_{CQ}.
[arus pemungut sepi, I_{CQ}]

(1 Mark/ *Markah*)

iii) quiescent collector-emitter voltage, V_{CEQ}.
[voltan pemungut- pemancar sepi , V_{CEQ}]

(2 Marks/ *Markah*)

iv) sketch the DC load line.
[Lakarkan garis beban DC.]

(5 Marks/ *Markah*)

Question 2
[Soalan 2]

Circuit in **Figure 2** shows a common emitter amplifier circuit with $\beta = 100$, $V_{BE(on)} = 0.7$ V, $V_T = 26\ mV$ and $V_A = \infty$.
*[Litar di **Rajah 2** menunjukkan satu litar penguat pemancar sepunya dengan $\beta = 100$, $V_{BE(on)} = 0.7$ V, $V_T = 26mV$ dan $V_A = \infty$.]*

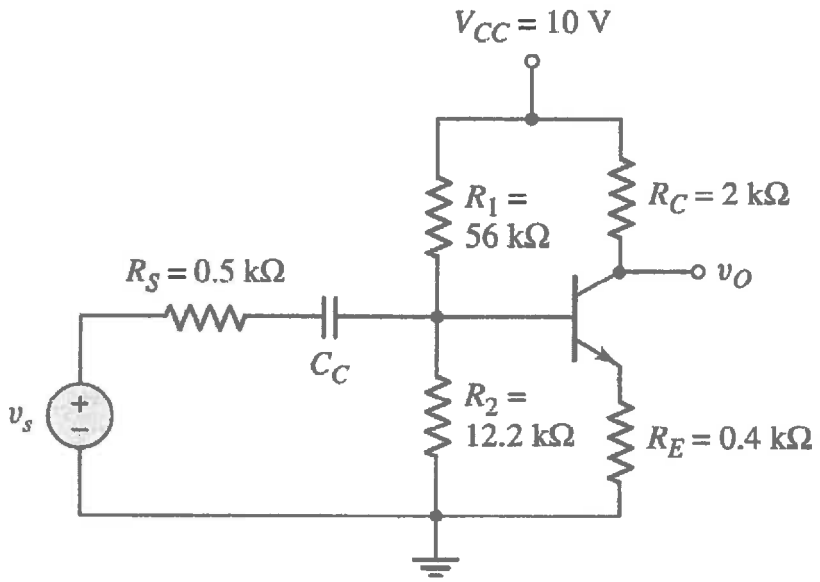

Figure 2
[Rajah 2]

(a) Based on **Figure 2**, determine;
*[Berpandukan pada **Rajah 2**, tentukan;]*

(i) base current, I_{BQ}.
[arus tapak , I_{BQ}]

(2 Marks/ *Markah*)

(ii) collector current, I_{CQ}.
[arus pemungut , I_{CQ}]

(1 Mark/ *Markah*)

(iii) collector-emitter voltage, V_{CE}.
[voltan pemancar-pemungut , V_{CE}]

(2 Marks/ *Markah*)

....5/-

(iv) draw small signal equivalent circuit.
[lukis litar setara isyarat kecil]

(5 Marks/ *Markah*)

(v) diffusion resistance, r_{π}.
[rintangan resapan, r_{π}.]

(2 Marks/ *Markah*)

(vi) transconductance, g_m.
[transkonduksian, gm.]

(2 Marks/ *Markah*)

(vii) input base resistance, R_{ib}.
[rintangan masukan tapak , R_{ib}.]

(2 Marks/ *Markah*)

(viii) input resistance to amplifier, R_i.
[rintangan masukan kepada litar penguat, R_i]

(2 Marks/ *Markah*)

(ix) small-signal voltage gain, A_v.
[gandaan voltan isyarat kecil, A_v.]

(2 Marks/ *Markah*)

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Question 3
[Soalan 3]

(a) Sketch the symbols for the both channels JFET.
[Lakarkan simbol bagi kedua-dua saluran JFET.]

(2 Marks/ *Markah*)

(b) Sketch and label the drain characteristic curve for JFET.
[Lakarkan dan labelkan lengkungan sifat pindahan bagi JFET.]

(3 Marks/ *Markah*)

(c) State **TWO (2)** types of JFET amplifiers.
[Nyatakan DUA (2) jenis penguat JFET.]

(2 Marks/ *Markah*)

(d) State **THREE (3)** advantages of FET devices.
[Nyatakan TIGA (3) kelebihan peranti FET.]

(3 Marks/ *Markah*)

(e) For the voltage divider bias JFET amplifier shown in **Figure 3(a)**, the transistor parameters are $I_{DSS} = 12mA$, *and* $V_{GS(OFF)} = -3V$. The transfer characteristic curve is given in the **Figure 3(b)**. Sketch a DC load line and determine the Q-point for the JFET circuit shown in **Figure 3(a)**.
*[Untuk penguat pincangan pembahagi voltan JFET yang ditunjukan di **Rajah 3(a)**, parameter transistor adalah $I_{DSS} = 12mA$ dan $V_{GS(OFF)} = -3V$. Lenkungan sifat pindahan diberi dalam **Rajah 3(b)**.Lakarkan garis beban DC dan tentukan titik-Q untuk litar JFET yang ditunjukkan dalam **Rajah 3(a)**.]*

(10 Marks/ *Markah*)

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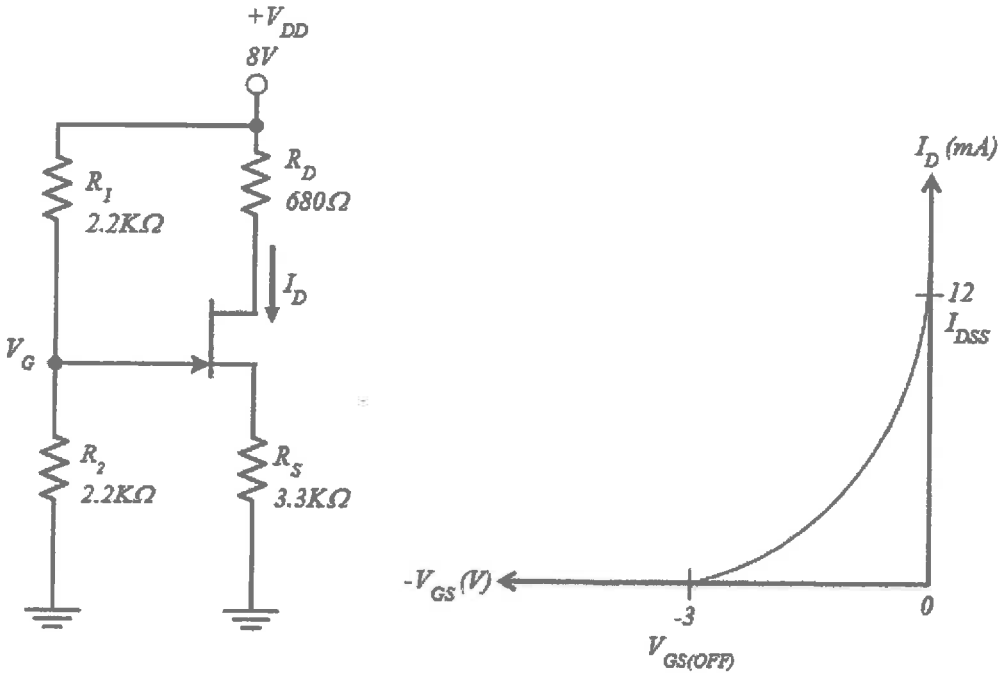

(a) (b)

Figure 3
[Rajah 3]

Question 4
[Soalan 4]

For the MOSFET amplifier in **Figure 4.1**, given the transistor parameter threshold voltage, $V_{TN} = 0.6\ V$, conduction parameter, $K_n = 0.5\ mA/V^2$, channel length modulation parameter, $\lambda = 0$, base resistance $R_1 = 1\ M\Omega$, base resistance $R_2 = 250\ k\Omega$, source resistance, $R_S = 2\ k\Omega$ and drain resistance, $R_D = 10\ k\Omega$.

*[Bagi penguat MOSFET dalam **Rajah 4.1**, diberi parameter-parameter bagi transistor adalah voltan ambang, $V_{TN} = 0.6\ V$, parameter pengaliran, $K_n = 0.5\ mA/V^2$, parameter modulatan panjang saluran, $\lambda = 0$, rintangan tapak $R_1 = 1\ M\Omega$, rintangan tapak $R_2 = 250\ k\Omega$, rintangan punca, $R_S = 2\ k\Omega$ dan rintangan salir $R_D = 10\ k\Omega$.]*

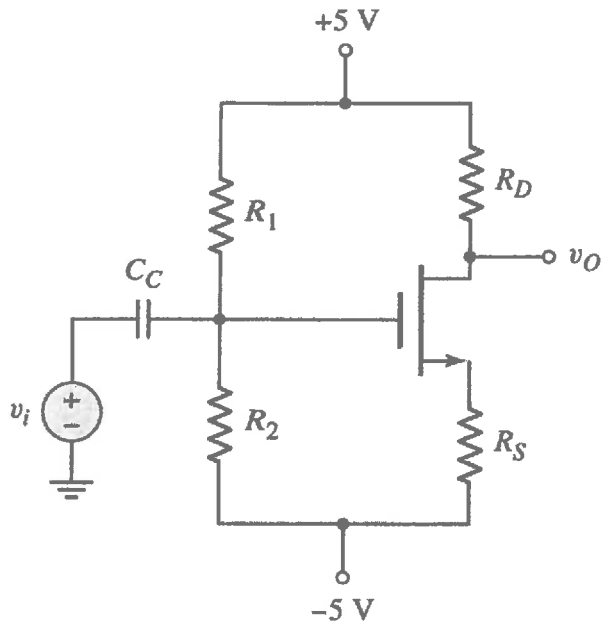

Figure 4.1
[*Rajah 4.1*]

(a) State the circuit configuration for **Figure 4.1.**
*[Nyatakan tatarajah lita r pada **Rajah 4.1**.]*

(1 Mark/ *Markah*)

(b) Based on **Figure 4.1**, determine;
*[Berdasarkan **Rajah 4.1**, tentukan;]*

(i) quiescent point (Q-point) values of I_{DQ} and V_{DSQ}.
[nilai-nilai titik sepi (titik-Q) bagi I_{DQ} and V_{DSQ}.]

(6 Marks/ *Markah*)

....9/-

(ii) small-signal voltage gain, A_v.
[gandaan voltan isyarat-kecil, A_v]

(2 Marks/ *Markah*)

(c) The transistor parameters for the circuit in **Figure 4.2** are $V_{TN} = 0.4V$, $K_n = 0.5\ mA/V^2$ *and* $\lambda = 0$. The circuit elements are $V_{DD} = 3V$ *and* $R_i = 300k\Omega$.
[*Parameter transistor bagi litar dalam* ***Rajah 4.2*** *adalah* $V_{TN} = 0.4V$, $K_n = 0.5mA/V^2$, $\lambda = 0$. *Elemen litar adalah* $V_{DD} = 3V$, *dan* $Ri = 300k\Omega$.]

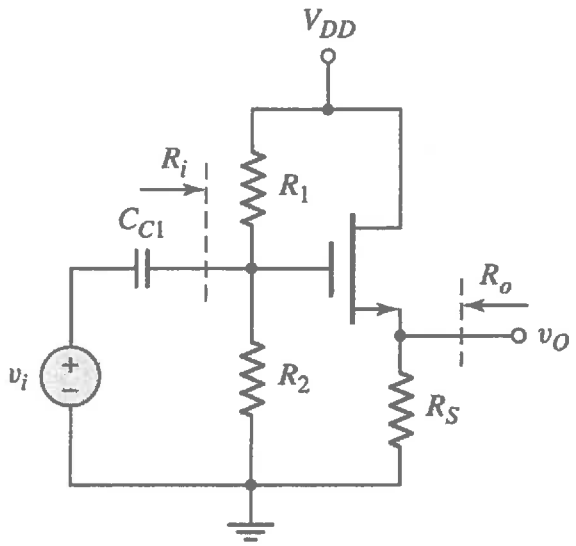

Figure 4.2
[***Rajah 4.2***]

(i) Design the circuit such that $I_{DQ} = 0.25\ mA$ and $V_{DSQ} = 1.5\ V$.
[*Rekabentuk litar supaya* $I_{DQ} = 0.25\ mA$ *dan* $V_{DSQ} = 1.5\ V$.]

(9 Marks/ *Markah*)

(ii) Determine the small-signal voltage gain, A_v.
[*Tentukan gandaan voltan isyarat-kecil,* A_v.]

(2 Marks/ *Markah*)

Section B
[Bahagian B]

Question 5
[Soalan 5]

Figure 5 shows a cascaded configuration as part of a multistage amplifier. The circuit elements transistor Q_1 and Q_2 are $\beta_1 = \beta_2 = 125$, $V_{BE(ON)} = 0.7V$ *and* $r_o = \infty$.
*[**Rajah 5** menunjukkan konfigurasi kaskad sebagai sebahagian daripada penguat berbilang tahap. Elemen-elemen transistor Q_1 dan Q_2 adalah $\beta 1 = \beta 2 = 125$, $V_{BE(ON)} = 0.7V$ and $r_o = \infty$.]*

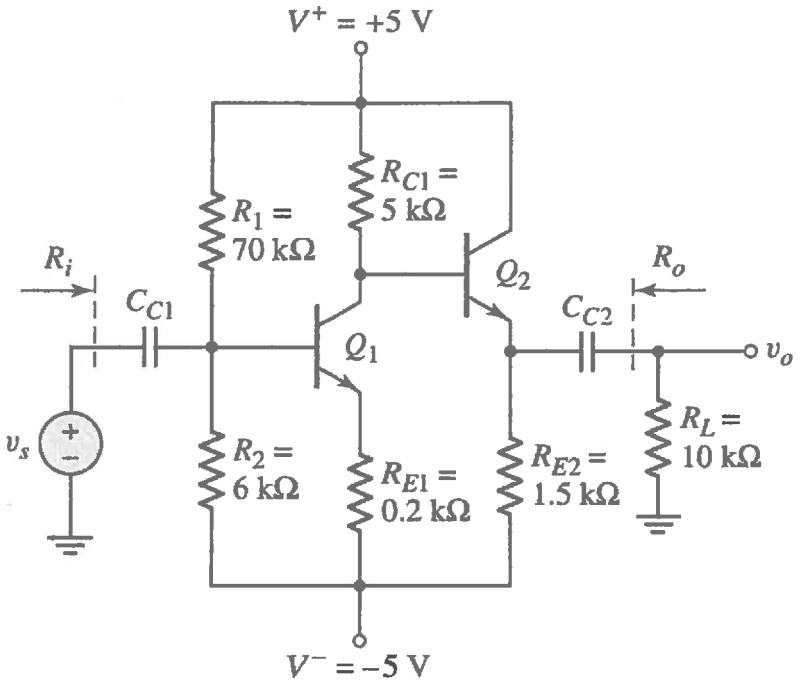

Figure 5
*[**Rajah 5**]*

(a) Based on **Figure 5**, determine;
*[Berpandukan **Rajah 5**, tentukan;]*

(i) thevenin resistor and voltage, R_{BB} *and* V_{BB}.
[voltan dan rintangan thevenin , R_{BB} dan V_{BB}]

(2 Marks/ *Markah*)

(ii) transistor Q_1 quiescent current, I_{BQ1}, I_{CQ1} and I_{EQ1}.
[arus sepi transistor Q_1 , I_{BQ1}, I_{CQ1} dan I_{EQ1}]

(3 Marks/ *Markah*)

....11/-

(iii) transistor Q_2 quiescent current, I_{BQ2}, I_{CQ2} and I_{EQ2}.
[arus sepi transistor Q_2 , I_{BQ2}, I_{CQ2} dan I_{EQ2}]

(3 Marks/ *Markah*)

(iv) transistor Q_1 voltage, V_{C1} and V_{E1}.
[voltan transistor Q_1 , V_{C1} dan V_{E1}]

(2 Marks/ *Markah*)

(v) transistor Q_2 voltage, V_{C2} and V_{E2}.
[voltan transistor Q_2 , V_{C2} dan V_{E2}]

(2 Marks/ *Markah*)

(vi) transistor Q_1 and Q_2 quiescent voltage, V_{CEQ1} and V_{CEQ2}.
[voltan sepi transistor Q_1 dan Q_2, V_{CEQ1} dan V_{CEQ2}]

(2 Marks/ *Markah*)

(b) Sketch small signal equivalent circuit for circuit configuration shown in **Figure 5.**
*[Lakarkan litar setara isyarat kecil bagi konfigurasi litar yang ditunjukkan dalam **Rajah 5.**]*

(6 Marks/ *Markah*)

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Question 6
[Soalan 6]

(a) Power amplifiers are generally classified according to the percent of time the output transistors are conducting. The four principal classifications are; class A, class B, class AB and class C. With the aid of diagram, sketch, label and define the collector current, ic versus time, ωt characteristics.
[Penguat-penguat kuasa dikelaskan secara umum mengikut peratus masa masa masukan pengaliran transistor. Empat pengkelasan utama adalah kelas A, kelas B, kelas AB dan kelas C. Dengan bantuan gambarajah, lakarkan, labelkan dan takrifkan ciri arus pemungut, ic melawan masa, ωt.]

i) Class A operation.
[Operasi kelas A.]

(2 Marks/ *Markah*)

ii) Class B operation.
[Operasi kelas B.]

(2 Marks/ *Markah*)

iii) Class AB operation.
[Operasi kelas AB.]

(2 Marks/ *Markah*)

iv) Class C operation.
[Operasi kelas C.]

(2 Marks/ *Markah*)

....13/-

(b) **Figure 6** shows a power amplifier configuration composed of complementary transistor pair Q_3 and Q_4. All transistor are assumed to be matched with $\beta = 60$ and $V_{BE(ON)} = V_{EB(ON)} = 0.6V$.

*[**Rajah 6** menunjukkan konfigurasi penguat kuasa yang terdiri daripada pasangan pelengkap transistor Q_3 dan Q_4. Kesemua transistor adalah dianggap sepadan dengan $\beta = 60$ dan $V_{BE(on)} = V_{EB(on)} = 0.6V$]*

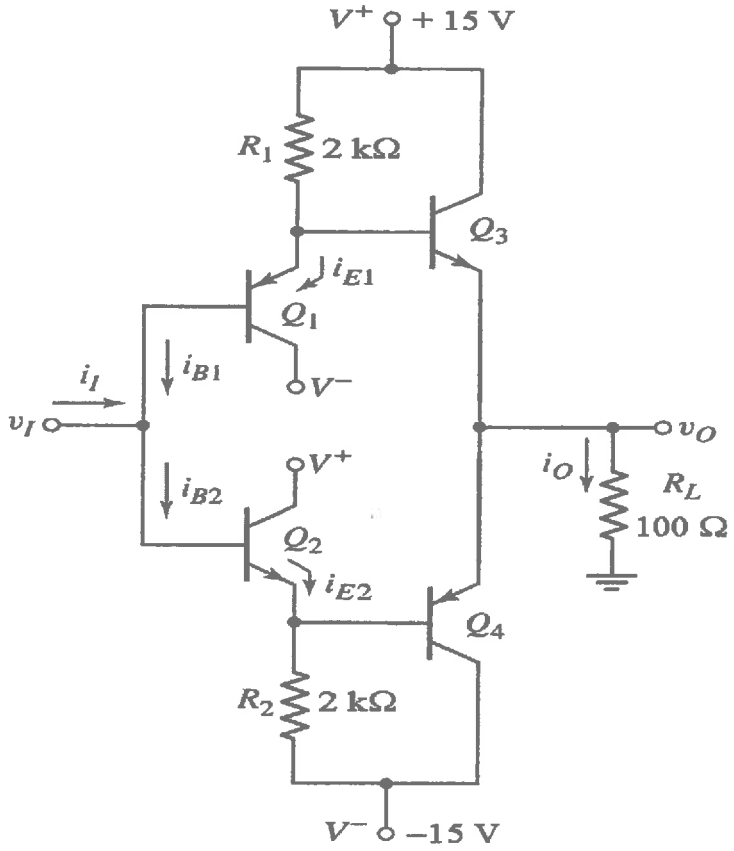

Figure 6
[Rajah 6]

(i) State the class of power amplifier configuration in **Figure 6**.
*[Nyatakan kelas bagi konfigurasi penguat kuasa dalam **Rajah 6**.]*

(1 Mark/ *Markah*)

(ii) For $V_I = 0V$, determine all the quiescent bias currents.
[Untuk $V_I = 0V$, tentukan semua arus-arus pincang sepi.]

(1 Mark/ *Markah*)

....14/-

(c) Based on **Figure 6**, for $V_1 = 10V$, determine the following;
*[Berdasarkan **Rajah 6**, untuk $V_1 = 10V$, tentukan yang berikut;]*

(i) output current, i_o.
[arus keluaran, io .]

(1 Mark/ *Markah*)

(ii) emitter current, I_{E3}.
[arus pemancar, I_{E3}.]

(1 Mark/ *Markah*)

(iii) base current, I_{B3}.
[arus tapak, I_{B3}.]

(1 Mark/ *Markah*)

(iv) current across R_1, I_{R1}.
[arus merentasi R_1, I_{R1}.]

(1 Mark/ *Markah*)

(v) emitter current, I_{E1}.
[arus pemancar, I_{E1}.]

(1 Mark/ *Markah*)

(vi) base current, I_{B1}.
[arus tapak, I_{B1}.]

(1 Mark/ *Markah*)

(vii) emitter current, I_{E2}.
[arus pemancar, I_{E2}.]

(1 Mark/ *Markah*)

(viii) base current, I_{B2}.
[arus tapak, I_{B2}.]

(1 Mark/ *Markah*)

(ix) input current, i_i.
[arus masukan, i_i.]

(1 Mark/ *Markah*)

(x) current gain, A_i.
[gandaan arus, A_i.]

(1 Mark/ *Markah*)

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Appendix A

[Lampiran A]

1. $g_m = \dfrac{I_{CQ}}{V_T}$
2. $r_{\Pi} = \dfrac{\beta V_T}{I_{CQ}}$
3. $g_m = 2K_n(V_{GS} - V_{TN})$
4. $g_m = \dfrac{2I_{DSS}}{|V_P|}\left(1 - \dfrac{V_{GS}}{V_P}\right)$
5. $A_v = -g_m R_C\left(\dfrac{r_\pi}{r_\pi + R_D}\right)$
6. $A_v = -g_m\left(\dfrac{R_1 \parallel R_2 \parallel r_\pi}{(R_1 \parallel R_2 \parallel r_\pi) + R_S}\right)(R_C \parallel r_o)$
7. $A_v = -\dfrac{\beta R_C}{r_\pi + (1+\beta)R_E}\left(\dfrac{R_i}{R_i + R_S}\right)$
8. $A_v = \dfrac{(1+\beta)(r_o \parallel R_E)}{r_\pi + (1+\beta)(r_o \parallel R_E)}\left(\dfrac{R_i}{R_i + R_S}\right)$
9. $A_v = g_m\left(\dfrac{R_C \parallel R_L}{R_S}\right)\left(\dfrac{r_\pi}{1+\beta} \parallel R_E \parallel R_S\right)$
10. $A_v = -g_m(r_o \parallel R_D)$
11. $A_v = \dfrac{-g_m(r_o \parallel R_D \parallel R_L)}{1 + g_m R_S}$
12. $A_v = -g_m(r_o \parallel R_D \parallel R_L)\left(\dfrac{R_i}{R_i + R_{Si}}\right)$
13. $A_v = \dfrac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}\left(\dfrac{R_i}{R_i + R_{Si}}\right)$
14. $A_v = \dfrac{g_m(r_o \parallel R_D \parallel R_L)}{1 + g_m R_{Si}}$
15. $A_v = -g_m(r_o \parallel R_D \parallel R_L)$
16. $A_v = \dfrac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}$
17. $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$
18. $I_D = K_N(V_{GS} - V_{TN})^2$
19. $V_{DS(sat)} = V_{GS} - V_{TN}$