UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Kedua
Sidang Akademik 2007/2008

21 April 2008

DMT 241 – Introduction To Integrated Circuit Layout
[Pengantar Bentangan Litar Terkamir]

Masa : 3 Jam

Please make sure that this question paper has **ELEVEN (11)** printed pages including this front page before you start the examination.
*[Sila pastikan kertas soalan ini mengandungi **SEBELAS (11)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This question paper has **SIX** questions. Answer any **FIVE** questions only.
*[Kertas soalan ini mengandungi **ENAM** soalan. Jawab mana-mana **LIMA** soalan sahaja.]*

Question 1

[Soalan 1]

(a) List **TWO (2)** advantages and disadvantages of Application Specific Integrated Circuits system.

[4 marks]

*[Senaraikan **DUA (2)** kelebihan dan kekurangan sistem litar terkamir beraplikasi spesifik.]*

[4 markah]

(b) List **THREE (3)** differences between Full Custom design and Field-Programmer Gate Arrays design.

[6 marks]

*[Senaraikan **TIGA (3)** perbezaan diantara rekabentuk binaan penuh dan rekabentuk 'Field-Programmer Gate Arrays'.]*

[6 markah]

(c) State **THREE (3)** operation regions for transistor.

[3 marks]

*[Nyatakan **TIGA (3)** kawasan operasi bagi transistor.]*

[3 markah]

(d) An NMOS transistor is in a 0.3 μm technology with W/L = 5/2. The gate oxide thickness for this process is 100 **Å**, the mobility of electrons is 350 cm^2/V.S and the threshold voltage is 0.7 V. Assume V_{dd} is equal to 5 V. Determine the operation region of NMOS if the value I_d across source to drain is 200 mA.

[7 marks]

[Satu transistor jenis NMOS berteknologi 0.35 μm dengan W/L = 5/2. Ketebalan get oksida bagi proses ini adalah 100 Å, pergerakkan elektron adalah 350 cm^2/V.S dan voltan ambang adalah 0.7 V. Andaikan V_{dd} bersamaan 5 V. Tentukan kawasan operasi bagi NMOS sekiranya nilai I_d merentasi punca ke salir adalah 200 mA.]

[7 markah]

Question 2

[Soalan 2]

(a) Briefly explain:

[Terangkan secara ringkas:]

(i) Transient Analysis **[2 marks]**

[Analisa transien] ***[2 markah]***

(ii) DC Analysis **[2 marks]**

[Analisa AT] ***[2 markah]***

(iii) AC Analysis **[2 marks]**

[Analisa AU] ***[2 markah]***

(b) Given $Q = A\overline{B} + \overline{A}B$:

[Diberikan $Q = A\overline{B} + \overline{A}B$ *:]*

(i) Write subckt netlist. **[7 marks]**

[Tuliskan netlist subckt.] ***[7 markah]***

(ii) Write a test-bench netlist using Piecewise Linear (PWL) source as an input signal.

[4 marks]

[Tuliskan netlist testbench menggunakan isyarat masukan Piecewise Linear (PWL) sebagai isyarat masukan.]

[4 markah]

(c) Refer to **Figure 2**, write the stimulus using PULSE as an input source.

[3 marks]

*[Rujuk kepada **Rajah 2**, tuliskan 'stimulus' mengunakan 'PULSE' sebagai sumber masukan.]*

[3 markah]

....4/-

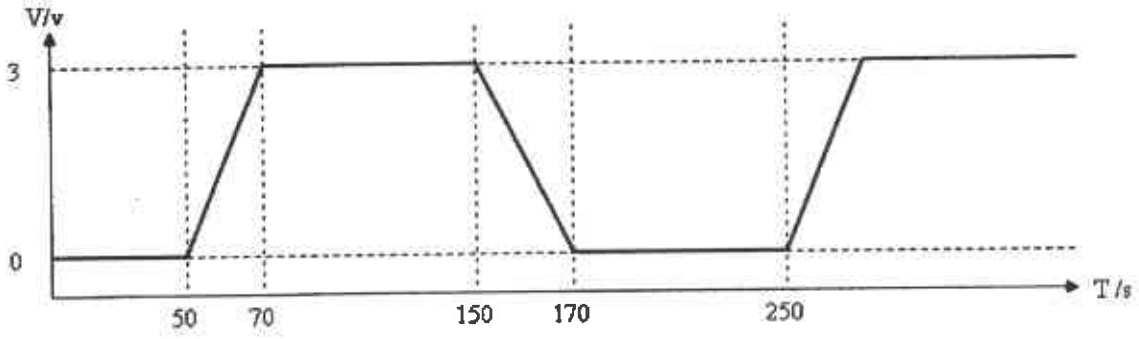

Figure 2

Rajah 2

Question 3

[Soalan 3]

(a) A 2:1 multiplexer can be developed by cascading **THREE (3)** 2-input NAND gates.

*[Satu pemultipleks 2:1 boleh dibina dengan melatakan **TIGA (3)** get TAK DAN 2-masukan.]*

(i) Sketch a block diagram for the 2:1 multiplexer. **[6 marks]**

[Lakarkan satu gambarajah blok untuk 2:1 pemultipleks.] ***[6 markah]***

(ii) Sketch the CMOS transistor level schematic circuit. **[10 marks]**

[Lakarkan litar skematik aras transistor CMOS.] ***[10 markah]***

(b) Design a 4:1 multiplexer by using the 2:1 multiplexer block diagram in part a (i). **[4 marks]**

[Rekabentukkan satu pemultipleks 4:1 dengan menggunakan gambarajah blok pemultipleks 2:1 daripada bahagian a(i).] ***[4 markah]***

Question 4

[Soalan 4]

(a) Sketch the corresponding transistor level schematic circuit in **Figure 4a** using:

*[Lakarkan skematik aras transistor berpandukan **Rajah 4a** dengan menggunakan:]*

(i) CMOS **[8 marks]**

[CMOS] ***[8 markah]***

(ii) Pseudo NMOS **[2 marks]**

[Pseudo NMOS] ***[2 markah]***

(b) Refer to **Figure 4b**. Complete the CMOS circuit based on PUN configuration. **[8 marks]**

*[Rujuk kepada **Rajah 4b**. Lengkapkan litar CMOS berdasarkan konfigurasi PUN.]*

[8 markah]

(c) Write the Boolean equation based on answer in part b. **[2 marks]**

[Tuliskan persamaan Boolean berdasarkan jawapan dalam bahagian b.]

[2 markah]

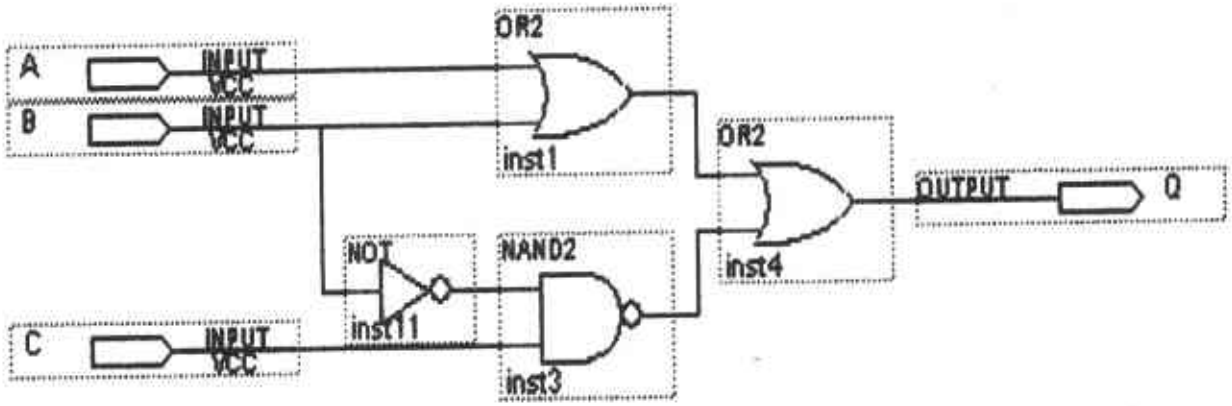

Figure 4a

Rajah 4a

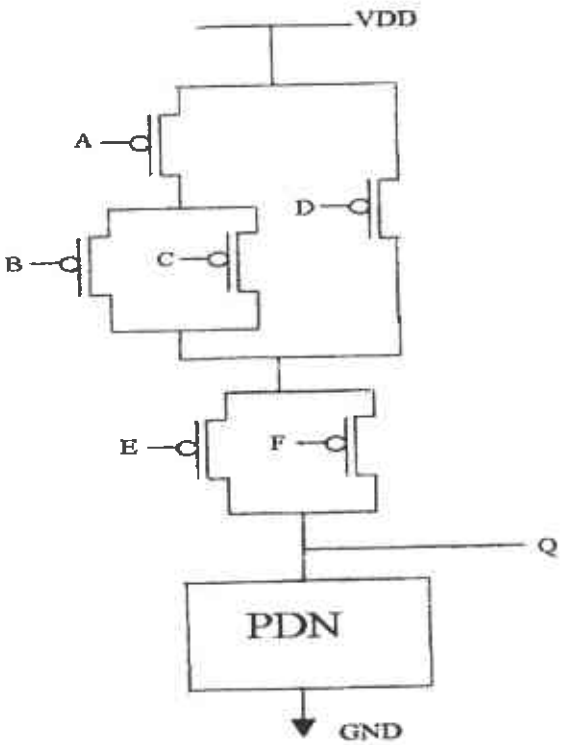

Figure 4b

Rajah 4b

Question 5

[Soalan 5]

(a) Refer to the layout shown in **Figure 5a**.

*[Rujuk kepada bentangan yang di tunjukkan di **Rajah 5a**.]*

(i) Sketch the stick diagram. **[3 marks]**

[Lakarkan rajah ranting.] ***[3 markah]***

(ii) Sketch the corresponding transistor level schematic circuit. **[7 marks]**

[Lakarkan litar skematik aras transistor yang sepadan.] ***[7 markah]***

(iii) Derive the Boolean equation for the circuit. **[2 marks]**

[Terbitkan persamaan Boolean bagi litar tersebut.] ***[2 markah]***

(b) Refer to the circuit in **Figure 5b:**

*[Rujuk kepada litar di **Rajah 5b:**]*

(i) Derive the Boolean equation. **[2marks]**

[Terbitkan persamaan Boolean.] ***[2 markah]***

(ii) Write the truth table for the circuit. **[6marks]**

[Tuliskan jadual kebenaran bagi litar tersebut.] ***[6 markah]***

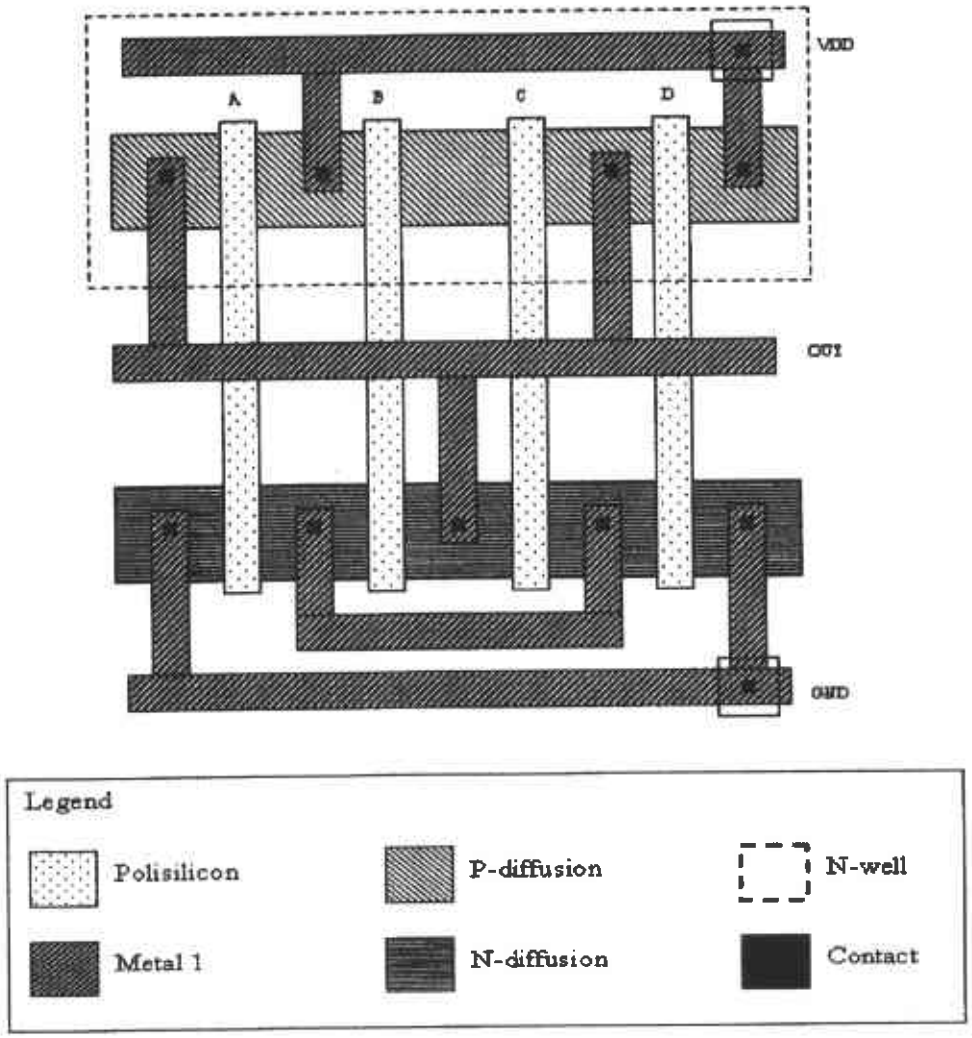

Figure 5a

Rajah 5a

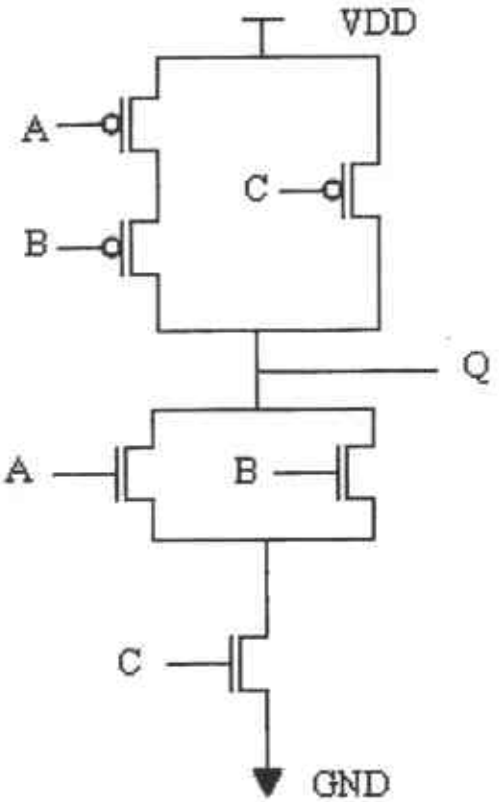

Figure 5b

Rajah 5b

Question 6

[Soalan 6]

(a) Refer to **Figure 6**:

*[Rujuk kepada **Rajah 6**:]*

(i) Sketch the Euler Path for the circuit. **[4 marks]**

[Lakarkan Laluan Euler bagi litar tersebut.] ***[4 markah]***

(ii) Sketch the stick diagram based on your answer in a(i). **[4 marks]**

[Lakarkan rajah ranting berdasarkan jawapan dalam a(i).] ***[4 markah]***

(iii) Draw the layout.based on 0.35 µm technology. Label the width and spacing.

[12 marks]

[Lukiskan bentangan berdasarkan technology 0.35 µm. labelkan lebar dan jarak.]

[12 markah]

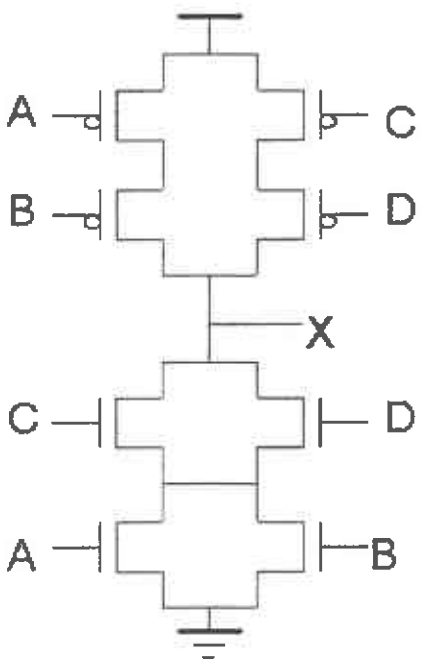

Figure 6

Rajah 6

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