

SULIT

UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Kedua
Sidang Akademik 2008/2009

27th April 2009

DMT 241 – Introduction To Integrated Circuit Layout
[Pengantar Bentangan Litar Terkamir]

Masa : 3 Jam

Please make sure that this question paper has **THIRTEEN (13)** printed pages including this front page before you start the examination.

*[Sila pastikan kertas soalan ini mengandungi **TIGA BELAS (13)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This question paper has **SIX (6)** questions. Answer **FIVE (5)** questions only.

*[Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab **LIMA (5)** soalan sahaja.]*

SULIT

Question 1

[Soalan 1]

- (a) List **THREE (3)** advantages of constructing digital circuit in integrated circuit (IC) compared to in the discrete components.
[Senaraikan TIGA (3) kelebihan pembinaan litar digital dalam litar terkamir(IC) berbanding dengan komponen diskerat.]
 (3 Marks / Markah)
- (b) Define Moore's Law and sketch the Moore's Law graph.
[Takrifkan Hukum Moore dan lakarkan graf nya.]
 (3 Marks / Markah)
- (c) Explain with the aid of a cross section diagram and an IV characteristic curve, the operation region for the NMOS transistor.
[Terangkan dengan bantuan suatu gambarajah keratan rentas dan suatu lengkung ciri IV, kawasan operasi bagi transistor NMOS.]
 (6 Marks / Markah)
- (d) An NMOS transistor designed using a $0.6 \mu\text{m}$ technology with gate oxide thickness (C_{ox}) of 100 \AA has a width of $6\mu\text{m}$ and a length of $2\mu\text{m}$, the mobility of electrons (μ_{N}) is $350 \text{ cm}^2/\text{V.S}$ and the threshold voltage is 0.7 V .
[Suatu transistor NMOS yang direkabentuk menggunakan teknologi $0.6 \mu\text{m}$ dengan ketebalan oksida get adalah 100 \AA mempunyai lebar $6\mu\text{m}$ dan panjang $2\mu\text{m}$, kebolehergerakan elektron adalah $350 \text{ cm}^2/\text{V.S}$ dan voltan ambang adalah 0.7 V .]
- i) Calculate C_{ox} and β for the transistor
[Kirakan C_{ox} dan β bagi transistor tersebut]
 (2 Marks / Markah)
- ii) Given the values of $V_{\text{gs}} = 0.3 \text{ V}, 3.3 \text{ V}, 5 \text{ V}$ and 8 V , calculate the corresponding I_{d} values for each V_{gs} when the transistor is operating in the saturation region.
[Diberi nilai- nilai V_{gs} adalah $0.3 \text{ V}, 3.3 \text{ V}, 5 \text{ V}$ dan 8 V . Kirakan nilai I_{d} bagi setiap V_{gs} apabila transistor beroperasi dalam keadaan tepu.]
 (4 Marks / Markah)
- iii) Determine the operating region of the NMOS transistor if the value of I_{d} , i.e. current from source to drain is 200 mA . Assume that V_{dd} is 5 V .
[Tentukan kawasan operasi bagi transistor NMOS tersebut sekiranya nilai I_{d} arus dari punca ke salir adalah 200 mA . Andaikan V_{dd} adalah 5 V .]
 (2 Marks / Markah)

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Question 2

[Soalan 2]

- (a) The SPICE simulator can perform various types of analysis on a circuit. For one of the analysis type, sketch a graph and briefly explain about the analysis.
[Penyelaku SPICE dapat menjalankan pelbagai jenis analisa terhadap litar. Bagi salah satu jenis analisa tersebut, lakarkan suatu graf dan terangkan secara ringkas mengenai analisa tersebut.]
(2 Marks / Markah)
- (b) Refer to **Figure 2**.
[Rujuk kepada Rajah 2.]
- (i) Write the Boolean equation for the output, OUT
[Tuliskan Persamaan Boolean untuk keluaran, OUT.]
(2 Marks / Markah)
- (ii) Write the netlist for the circuit.
[Tuliskan "netlist" bagi litar tersebut.]
(3 Marks / Markah)
- (iii) Write a test-bench netlist using Piecewise Linear (PWL) source as the input signal.
[Tuliskan "netlist" "testbench" menggunakan Piecewise Linear (PWL) sebagai isyarat-isyarat masukan.]
(3 Marks / Markah)

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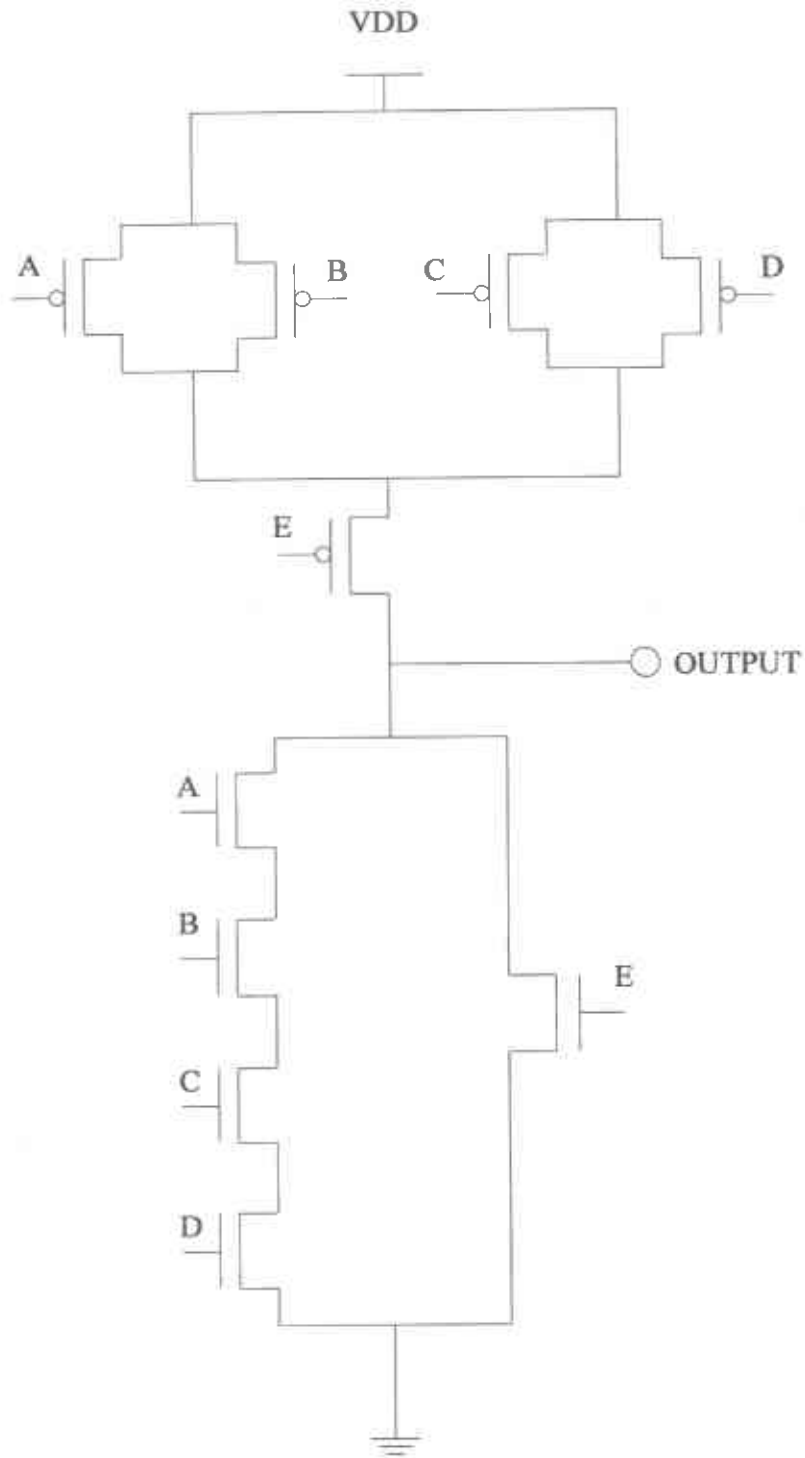


Figure 2
[Rajah 2]

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(c) Given $X = \overline{\overline{AB} + \overline{CD}}$.

[Diberi $X = \overline{\overline{AB} + \overline{CD}}$.]

- (i) Simplify the Boolean equation
[Permudahkan persamaan Boolean] (2 Marks / Markah)
- (ii) Sketch the gate level schematic for the equation.
[Lakarkan skematik aras get bagi persamaan tersebut] (2 Marks / Markah)
- (iii) Sketch the transistor level schematic for the equation
[Lakarkan skematik aras transistor bagi persamaan tersebut] (3 Marks / Markah)
- (iv) Write the Netlist for the equation
[Tuliskan "netlist" bagi persamaan tersebut.] (3 Marks / Markah)

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Question 3

[Soalan 3]

Figure 3 shows a combinational logic gates. It consists of a AND gate and two OR gates.

[Rajah 3 menunjukkan sebuah kombinasi get logik. Ianya terdiri daripada satu get DAN dan dua get ATAU.]

- (a) Write the Boolean equation for the output, D
[Tuliskan Persamaan Boolean untuk keluaran, D.] (2 Marks / Markah)
- (b) Sketch the CMOS transistor level schematic circuit.
[Lakarkan litar skematik aras transistor CMOS] (4 Marks / Markah)
- (c) Write a netlist for the circuit
[Tuliskan suatu "netlist" bagi litar tersebut.] (3 Marks / Markah)
- (d) Sketch the pseudo-NMOS transistor level schematic circuit.
[Lakarkan litar skematik aras transistor pseudo-NMOS] (3 Marks / Markah)
- (e) Sketch the stick diagram for the circuit.
[Lakarkan rajah ranting untuk litar tersebut.] (5 Marks / Markah)
- (f) Based on your Boolean equation in (a), derive a truth table for the circuit.
[Berdasarkan persamaan Boolean pada (a), terbitkan jadual kebenaran bagi litar tersebut.] (3 Marks / Markah)

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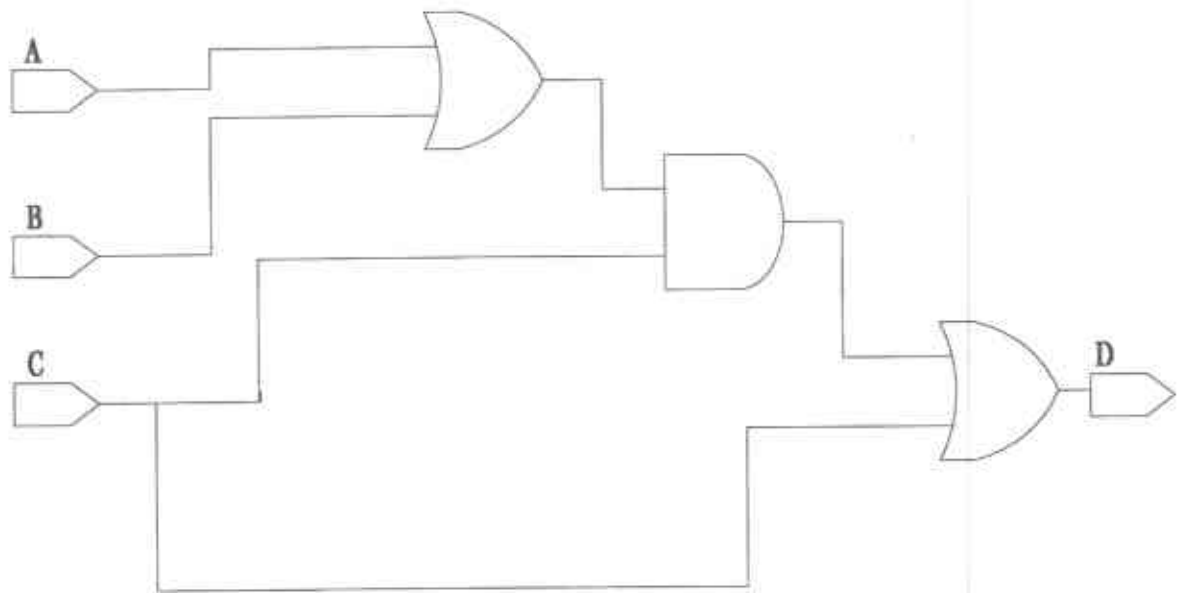


Figure 3
[Rajah 3]

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Question 4**[Soalan 4]**

- (a) State the main reason why an IC designer performs Design Rules Check (DRC) on a layout.
[Nyatakan sebab utama mengapa perekabentuk litar terkamir menjalankan semakan aturan rekabentuk (DRC) terhadap suatu bentangan.]
(2 Marks / Markah)
- (b) Refer to **Figure 4**.
[Rujuk Rajah 4.]
- (i) Find the Boolean expression for the output, W.
[Cari persamaan Boolean bagi keluaran, W.]
(2 Marks / Markah)
- (ii) Sketch an Euler path for the circuit.
[Lakarkan laluan Euler bagi litar tersebut.]
(2 Marks / Markah)
- (iii) Sketch a stick diagram based on your answer in (i).
[Lakarkan rajah ranting berdasarkan jawapan di (i).]
(4 Marks / Markah)
- (c) Draw the physical layout for the NAND gate using graph paper provide.
[Lukiskan bentangan fizikal bagi suatu get TAK DAN dengan menggunakan kertas graf yang di sediakan.]
(10 Marks / Markah)

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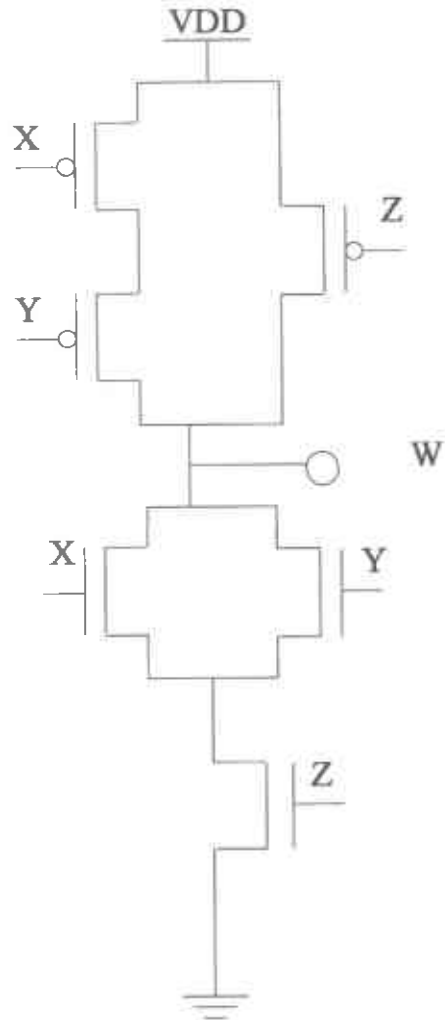


Figure 4
[Rajah 4]

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Question 5*[Soalan 5]*

- (a) Explain briefly the operation of pseudo-NMOS Logic circuit.
[Terangkan secara ringkas operasi litar logik pseudo-NMOS.]
(2 Marks / Markah)
- (b) Based on **Figure 5 (a)**,
[Berdasarkan Rajah 5 (a),]
- (i) Write the Boolean equation for the output, F.
[Tuliskan persamaan Boolean bagi keluaran, F.]
(2 Marks / Markah)
- (ii) Sketch the transistor-level schematic using Complementary CMOS logic.
[Lakarkan skematik aras-transistor dengan menggunakan logik pelengkap CMOS.]
(4 Marks / Markah)
- (iii) Sketch the transistor-level schematic using pseudo-NMOS.
[Lakarkan skematik aras-transistor dengan menggunakan pseudo-NMOS.]
(3 Marks / Markah)
- (c) **Figure 5 (b)** shows a layout of a combinational logic gate. Based on the figure:
[Rajah 5(b) menunjukkan satu bentangan untuk kombinasi get logik. Berdasarkan pada rajah tersebut:]
- (i) Sketch a stick diagram for the layout.
[Lakarkan rajah ranting bagi bentangan tersebut.]
(5 Marks / Markah)
- (ii) Sketch the corresponding transistor-level schematic.
[Lakarkan skematik aras-transistor yang sepadan.]
(4 Marks / Markah)

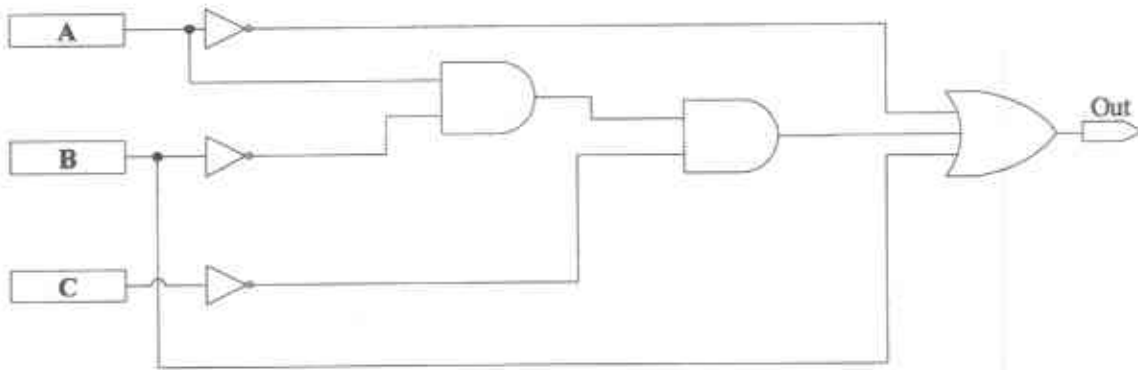


Figure 5 (a)

[Rajah 5 (a)]

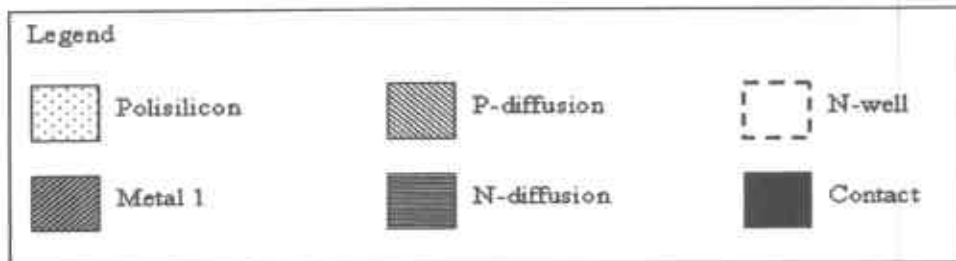
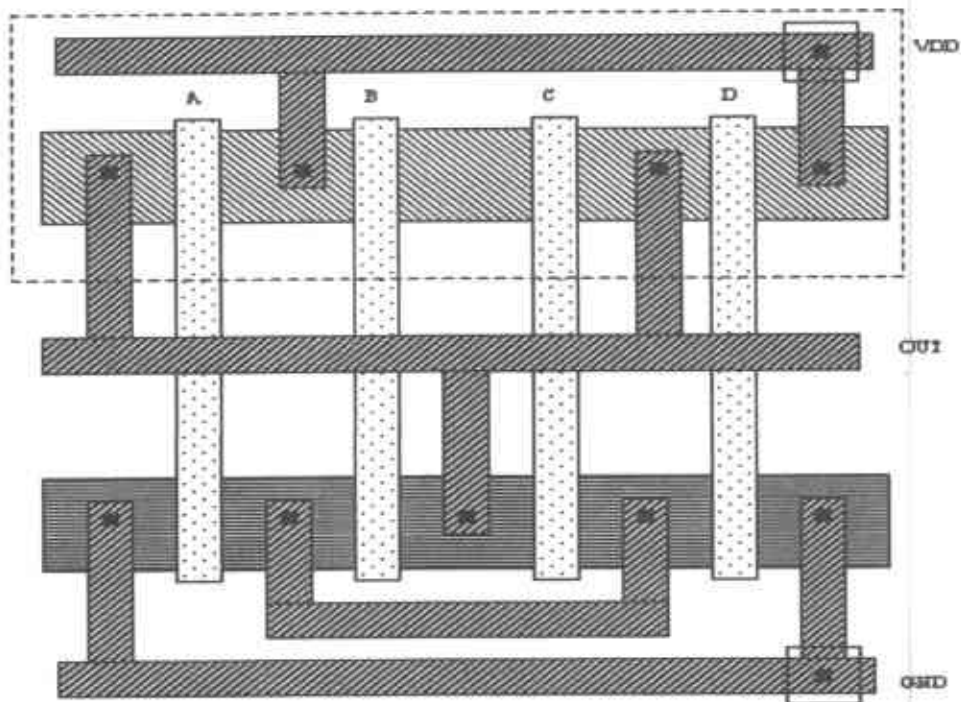


Figure 5 (b)

[Rajah 5 (b)]

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Question 6

[Soalan 6]

- (a) What is the difference between Static CMOS and Dynamic CMOS?
[Apakah perbezaan antara CMOS statik dan CMOS dinamik?]
(2 Marks / Markah)
- (b) List **TWO (2)** advantages and **ONE (1)** disadvantage of pseudo-NMOS.
[Senaraikan DUA (2) kebaikan dan SATU (1) kekurangan pseudo-NMOS.]
(3 Marks / Markah)
- (c) Explain briefly with the aid of a diagram:.
[Terangkan secara ringkas dengan bantuan gambarajah.]
- (i) The operation of a Pull Down Network (PDN) using NMOS transistor.
[Operasi Jaringan Tolakan Bawah (PDN) menggunakan transistor NMOS.]
(2 Marks / Markah)
- (iii) The operation of a Pull Up Network (PUN) using PMOS transistor.
[Operasi Jaringan Tolakan Atas (PUN) menggunakan transistor PMOS.]
(2 Marks / Markah)
- (iii) The operation of a Dynamic Logic circuit.
[Operasi di dalam suatu litar Logik Dinamik.]
(2 Marks / Markah)
- (d) Refer to **Figure 6**.
[Rujuk kepada Rajah 6.]
- (i) Complete the PDN of the Complementary CMOS circuit based on PUN configuration.
[Lengkapkan litar Pelengkap CMOS PDN berdasarkan konfigurasi PUN tersebut.]
(4 Marks / Markah)
- (iii) Sketch a stick diagram for the whole circuit.
[Lakarkan suatu rajah ranting untuk keseluruhan litar.]
(5 Marks / Markah)

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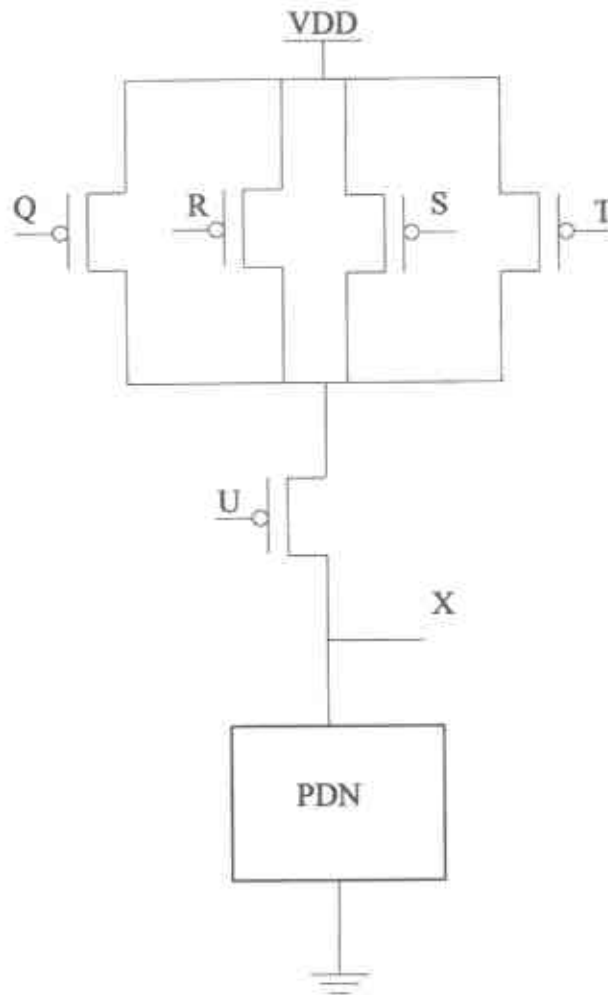


Figure 6
[Rajah 6]

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