UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Kedua
Sidang Akademik 2013/2014

14 Mac 2014

DMT 241 – Introduction To Integrated Circuit Layout
[Pengantar Bentangan Litar Terkamir]

Please make sure that this question paper has **FOURTEEN (14)** printed pages including this front page before you start the examination.
*[Sila pastikan kertas soalan ini mengandungi **EMPAT BELAS (14)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This question paper has **SIX (6)** questions. Answer **any FIVE (5)** questions only. Each question contributes 20 marks.
*[Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab **mana-mana LIMA (5)** soalan sahaja. Markah bagi tiap-tiap soalan adalah 20 markah.]*

Please answer Question 1(b) (iv) by using the answer sheet in **Appendix I**.
*[Sila jawab Soalan 1(b)(iv) dengan menggunakan kertas jawapan dalam **Lampiran I**.]*

Dicetak oleh Unit Peperiksaan & Pengijazahan, Bahagian Pengurusan Akademik, Jabatan Pendaftar.

Question 1
[Soalan 1]

(a) Integrated Circuit (IC) is a complex set of electronic components where their interconnections are etched or imprinted onto a tiny slice of semiconducting material.
[Litar Bersepadu (IC) ialah satu kumpulan komplek komponen elektronik di mana saling hubungannya dipunar atau dicetak ke atas satu potongan kecil bahan separa pengalir.]

(i) State **TWO (2)** advantages of IC.
[Nyatakan DUA (2) kelebihan IC.]

(2 Marks/ *Markah*)

(ii) List the IC design flow.
[Senaraikan aliran rekabentuk IC.]

(4 Marks/ *Markah*)

(b) Refer to the SPICE netlist in **Figure 1(b)(i):**
*[Rujuk kepada "netlist" SPICE dalam **Rajah 1(b)(i):**]*

```
.subckt Ques1b      P     Q     R     OUT
      MP1  N1   P     VDD   VDD   p     L=2u  W=5u
      MP2  N1   Q     VDD   VDD   p     L=2u  W=5u
      MP3  OUT  R     N1    VDD   p     L=2u  W=5u
      MN1  OUT  P     N2    GND   n     L=2u  W=5u
      MN2  N2   Q     GND   GND   n     L=2u  W=5u
      MN3  OUT  R     GND   GND   n     L=2u  W=5u
.ends Ques1b
```

Figure 1(b)(i)
[Rajah 1(b)(i)]

(i) Sketch the schematic circuit.
[Lakarkan litar skematik.]

(4 Marks/ *Markah*)

(ii) Write the equation for the output, *OUT*.
[Tuliskan persamaan untuk keluaran, OUT.]

(2 Marks/ *Markah*)

....3/-

(iii) Write a testbench with source as an input signal in **Figure 1(b)(ii)** by using Piecewise Linear (PWL).
*[Tulis satu "testbench" dengan sumber sebagai satu isyarat input dalam **Rajah 1 (b)(ii)** dengan menggunakan Piecewise Linear (PWL).]*

(6 Marks/ *Markah*)

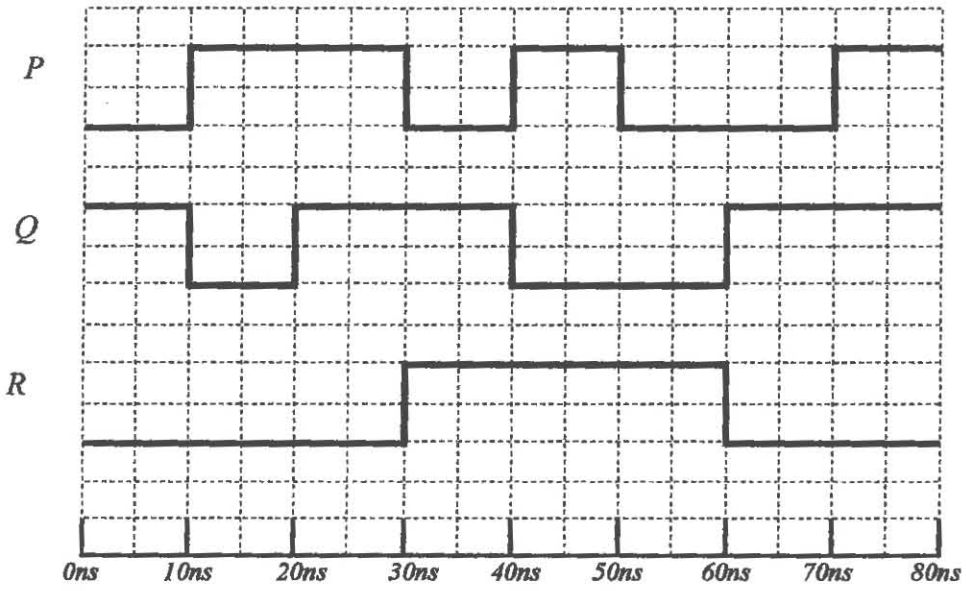

Figure 1(b)(ii)
[Rajah 1(b)(ii)]

(iv) Sketch the output waveform, *OUT* in **Appendix I**.
*[Lakarkan gelombang keluaran, OUT dalam **Lampiran I**.]*

(2 Marks/ *Markah*)

Question 2
[Soalan 2]

(a) In year 1965, Gordon Moore predicted that the transistors count doubled every 18 months per chip. From year 1976 to 2006, the number of transistor increased from one thousand transistors to one million transistors. From Moore's Law ;
[Dalam tahun 1965, Gordon Moore meramalkan kiraan transistor bertambah dua kali ganda setiap 18 bulan per cip. Dari tahun 1976 hingga 2006, bilangan transistor meningkat dari seribu transistor ke sejuta transistor. Daripada Hukum Moore ;]

(i) sketch the Moore's Law graph.
[lakarkan graf Hukum Moore.]

(2 Marks/ *Markah*)

(ii) list **FOUR (4)** integration levels that reflect to Moore's Law in term of gate count.
*[senaraikan **EMPAT (4)** tahap pengamiran yang mencerminkan Hukum Moore dari segi kiraan get.]*

(4 Marks/ *Markah*)

(iii) explain the evolution of IC technology in industry.
[terangkan evolusi teknologi IC dalam industri .]

(2 Marks/ *Markah*)

(b) Based on **Figure 2(b)(i):**
*[Berdasarkan **Rajah 2(b)(i):**]*

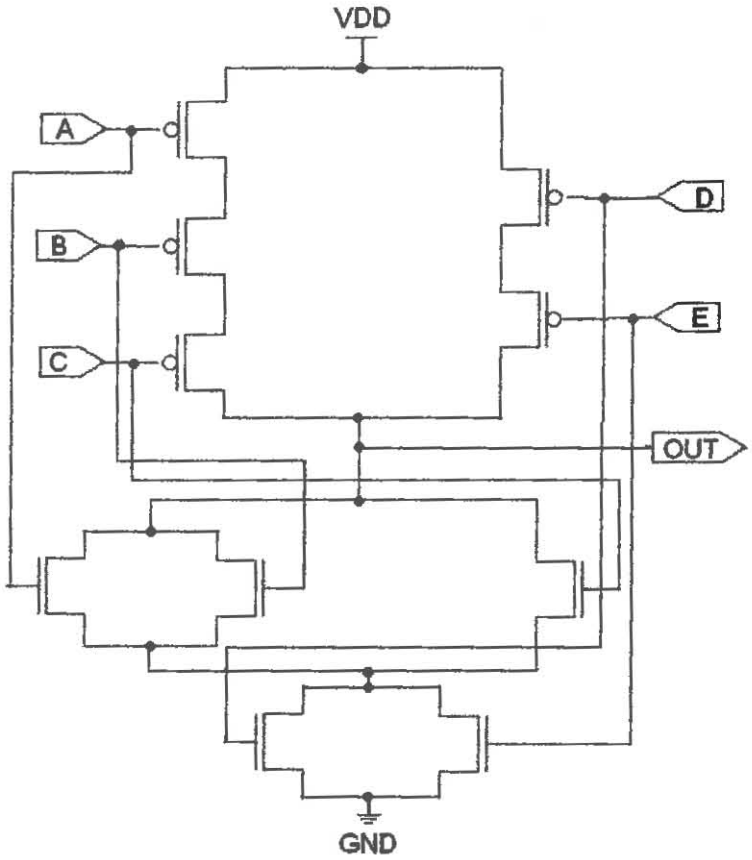

Figure 2(b)(i)
[Rajah 2(b)(i)]

(i) Identify the Boolean equation for output, OUT.
[Kenalpasti persamaan Boolean bagi keluaran, OUT.]

(2 Marks/ *Markah*)

(ii) Write the SPICE netlist.
[Tuliskan "netlist" SPICE.]

(6 Marks/ *Markah*)

....6/-

(iii) Write a testbench using PULSE source as the input signal in **Figure 2(b)(ii)**.
*[Tuliskan "testbench" menggunakan sumber DEDENYUT sebagai isyarat masukan dalam **Rajah 2(b)(ii)**.]*

(4 Marks/ *Markah*)

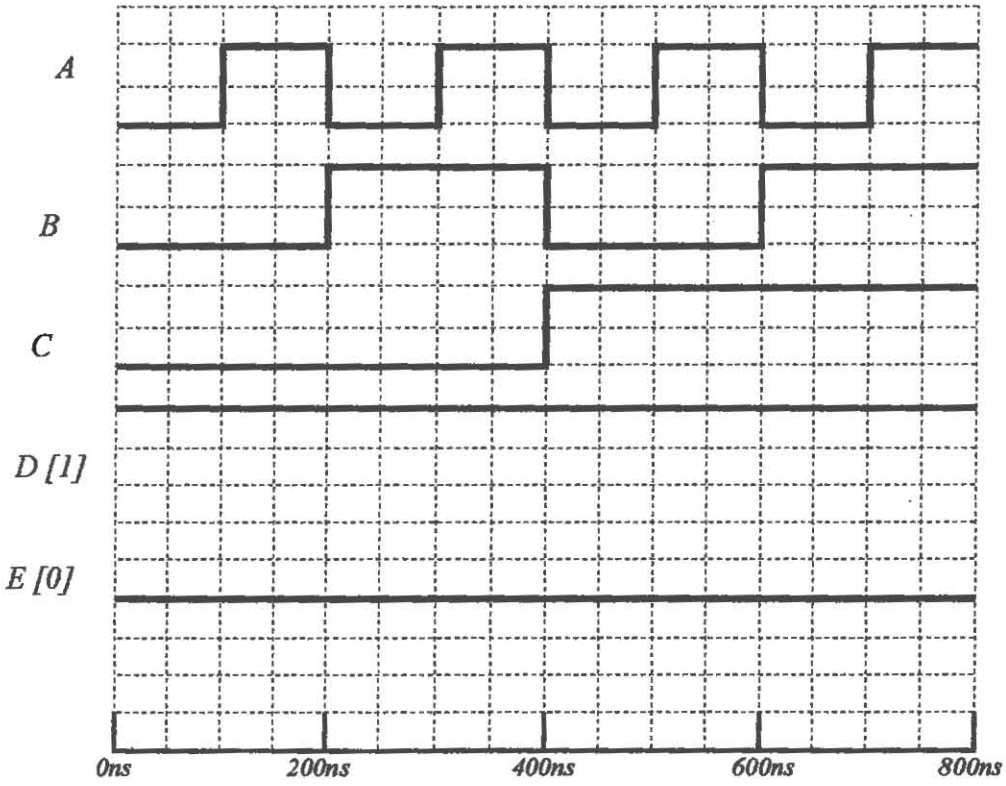

Figure 2(b)(ii)
[Rajah 2(b)(ii)]

Question 3
[Soalan 3]

(a) A Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has two ohmic contacts (source and drain). The number of charges in the channel is controlled by a third contact (gate) where conducting channel is formed when sufficient voltage is applied. With the aid of diagram, briefly explain:
[Satu Transistor Kesan Medan Separuh Pengalir-Oksida-Logam (MOSFET) mengandungi dua sentuhan ohm (sumber dan salir). Jumlah pembawa cas di saluran dikawal oleh satu hubungan ketiga (get) di mana salur pngalir terbentuk apabila voltan secukupnya diberikan. Dengan bantuan gambarajah, terangkan:]

(i) accumulation mode.
[mod pengumpulan.]

(3 Marks/ *Markah*)

(ii) depletion mod.
[mod kesusutan.]

(3 Marks/ *Markah*)

(iii) inversion mod.
[mod songsangan.]

(3 Marks/ *Markah*)

....8/-

(b) Refer **Figure 3(b):**
*[Rujuk **Rajah 3(b):**]*

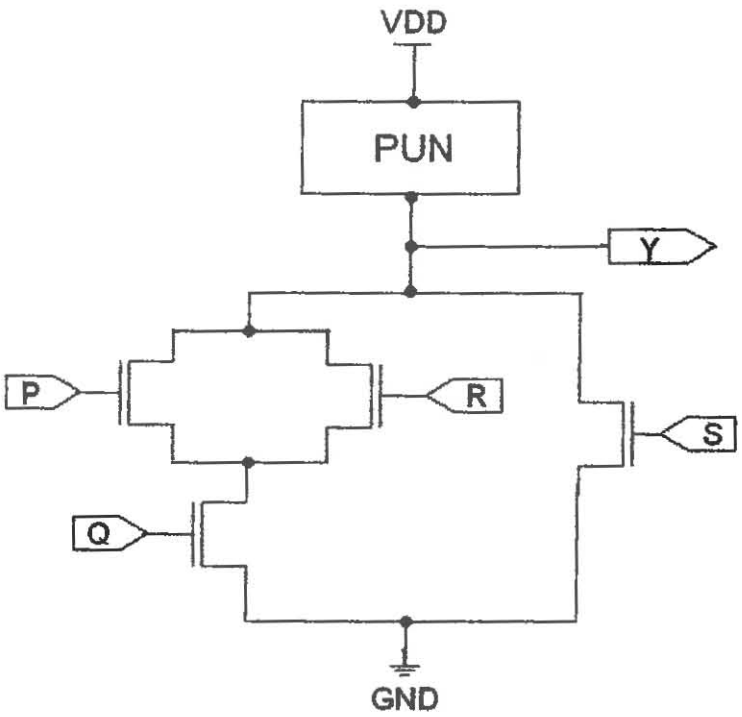

Figure 3(b)
[Rajah 3(b)]

(i) Illustrate the Pull-Up Network (PUN) of the CMOS circuit based on Pull Down Network (PDN) configuration.
[Ilustrasikan Rangkaian Tarik-Atas (PUN) untuk litar CMOS berdasarkan konfigurasi Rangkaian Tarik-Bawah (PDN).]

(2 Marks/ *Markah*)

(ii) Find the Boolean equation for the output, Y.
[Cari persamaan Boolean bagi keluaran, Y.]

(1 Mark/ *Markah*)

(iii) Sketch the Eular path for the circuit.
[Lakarkan laluan Eular bagi litar tersebut.]

(2 Marks/ *Markah*)

(iv) Sketch a stick diagram based on answer in 3(b)(iii)
[Lakarkan satu gambarajah ranting berdasarkan jawapan di 3(b)(iii).]

(6 Marks/ *Markah*)

Question 4
[Soalan 4]

(a) Application Specific Integrated Circuit (ASIC) is an integrated circuit customized for a particular application.
[Aplikasi Tertentu Litar Bersepadu (ASIC) adalah satu litar bersepadu yang disesuaikan untuk aplikasi tertentu.]

(i) List **FOUR (4)** types of ASIC design methodologies.
*[Senaraikan **EMPAT (4)** jenis rekabentuk metodologi ASIC.]*

(2 Marks/ *Markah*)

(ii) Discuss **TWO (2)** advantages and disadvantages of ASIC system.
*[Bincangkan **DUA (2)** kelebihan dan kekurangan sistem ASIC.]*

(4 Marks/ *Markah*)

(b) **Figure 4** shows a combinational logic gates. It consists of an OR gate and a NAND gate. Based on the figure, sketch;
*[**Rajah 4** menunjukkan sebuah kombinasi get logik. Ianya terdiri daripada satu get ATAU dan satu get TAK-DAN.Berdasarkan rajah, lakarkan;]*

(i) the CMOS transistor level schematic circuit.
[litar skematik aras transistor CMOS.]

(3 Marks/ *Markah*)

(ii) the Euler path.
[laluan Euler.]

(2 Marks/ *Markah*)

(iii) the layout for the circuit.
[bentangan bagi litar.]

(9 Marks/ *Markah*)

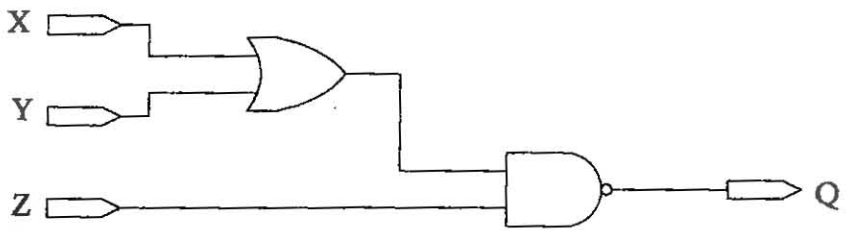

Figure 4
[Rajah 4]

Question 5
[Soalan 5]

(a) Based on nMOS transistor;
[Berdasarkan transistor nMOS;]

(i) State **THREE (3)** operation regions.
[Nyatakan TIGA (3) kawasan operasi.]

(3 Marks/ *Markah*)

(ii) Sketch the graph of I-V characteristics.
[Lakarkan graf ciri-ciri I-V.]

(2 Marks/ *Markah*)

(b) The nMOS transistor is designed with (W/L) = 8, the gate oxide thickness, t_{ox} = 180 Å, the mobility of electrons, μ_n = 520 cm^2/V-s and the threshold voltage, V_{Tn} = 0.75V. Given $\mathcal{E}_o = 8.854 \times 10^{-14}$ F/cm.
[Transistor nMOS direkabentuk dengan (W/L) = 8, ketebalan oksida get, t_{ox} = 180 Å, kebolehgerakan elektron, μ_n = 520 cm^2/V-s dan voltan ambang, V_{Tn} = 0.75V. Diberi $\mathcal{E}_o = 8.854 \times 10^{-14}$ F/cm.]

(i) Calculate gate oxide capacitance, C_{ox} and β for the transistor.
[Kirakan kemuatan get oksida, C_{ox} dan β bagi transistor.]

(3 Marks/ *Markah*)

(ii) Analyze the operating region for the transistor if V_{GS} = 0.5V; V_{DS} = 2V with V_{GS} = 2V; and V_{DS} = 1.2V with V_{GS} = 2V.
[Analisa kawasan operasi bagi transistor jika V_{GS} = 0.5V; V_{DS} = 2V dengan V_{GS} = 2V; dan V_{DS} = 1.2V dengan V_{GS} = 2V.]

(3 Marks/ *Markah*)

(iii) Calculate the corresponding drain current, I_d by referring the answer in 5(b)(ii).
[Kirakan arus saliran, I_d dengan merujuk jawapan dalam 5(b)(ii).]

(3 Marks/ *Markah*)

(c) Based on the stick diagram in **Figure 5** below, answer the following questions:
*[Berdasarkan gambarajah ranting dalam **Rajah 5** di bawah, jawab soalan-soalan berikut:]*

(i) Construct the equivalent CMOS schematic diagram.
[Binakan gambarajah skematik setara CMOS.]

(4 Marks/ *Markah*)

(ii) Express the Boolean equation for CMOS schematic diagram.
[Nyatakan ungkapan Boolean bagi gambarajah skematik CMOS.]

(2 Marks/ *Markah*)

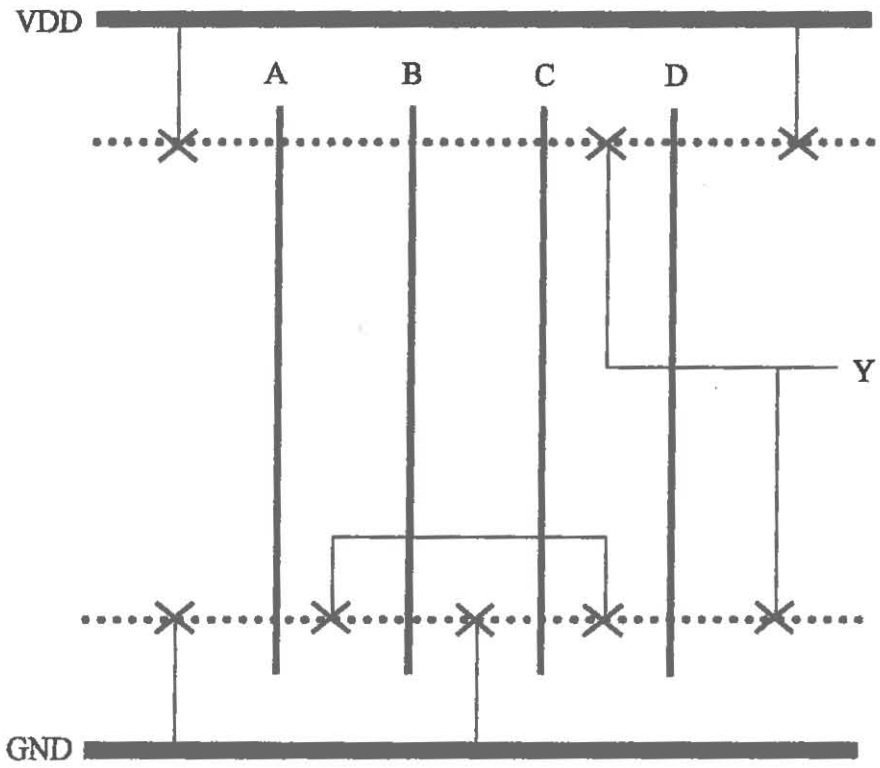

Figure 5
[Rajah 5]

Question 6
[Soalan 6]

(a) (i) Sketch and label the physical structure of pMOS and nMOS transistors respectively.
[Lakar dan labelkan struktur fizikal bagi transistor pMOS dan nMOS masing-masing.]
(4 Marks/ *Markah*)

(ii) With aid of a diagram, sketch and explain the flow of currents in transistor to be viewed as a simple ON/OFF switches for inverter.
[Dengan bantuan gambarajah, lakar dan terangkan aliran arus dalam transistor untuk dilihat sebagai suis ringkas BUKA/TUTUP bagi penyongsang.]
(4 Marks/ *Markah*)

(b) Given the layout diagram as shown in **Figure 6.**
*[Diberi gambarajah bentangan seperti dalam **Rajah 6.**]*

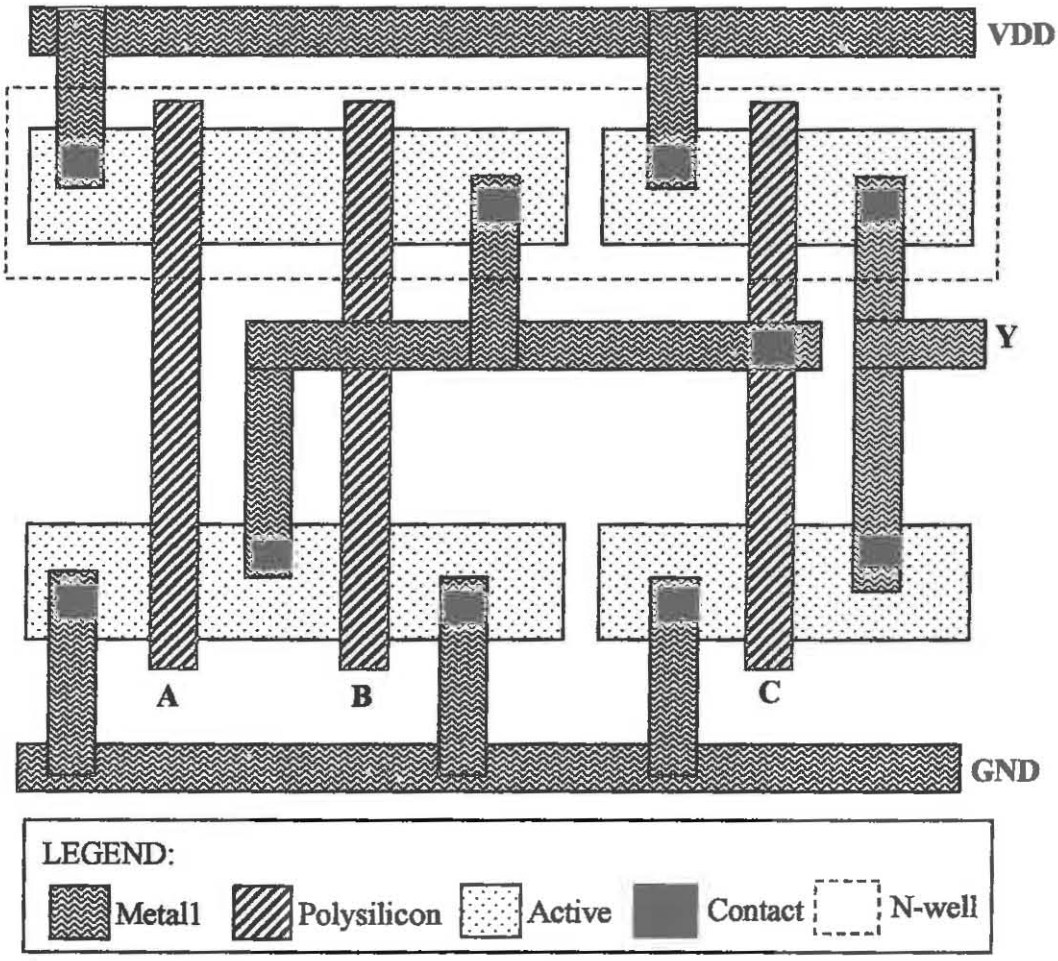

Figure 6
[Rajah 6]

....13/-

(i) Sketch the stick diagram.
[Lakarkan gambarajah ranting.]

(7.5 Marks/ *Markah*)

(ii) Sketch the CMOS transistor level schematic.
[Lakarkan litar skematik aras transistor CMOS.]

(3.5 Marks/ *Markah*)

(iii) Determine the Boolean equation.
[Tentukan persamaan Boolean.]

(1 Mark/ *Markah*)

-ooOoo-

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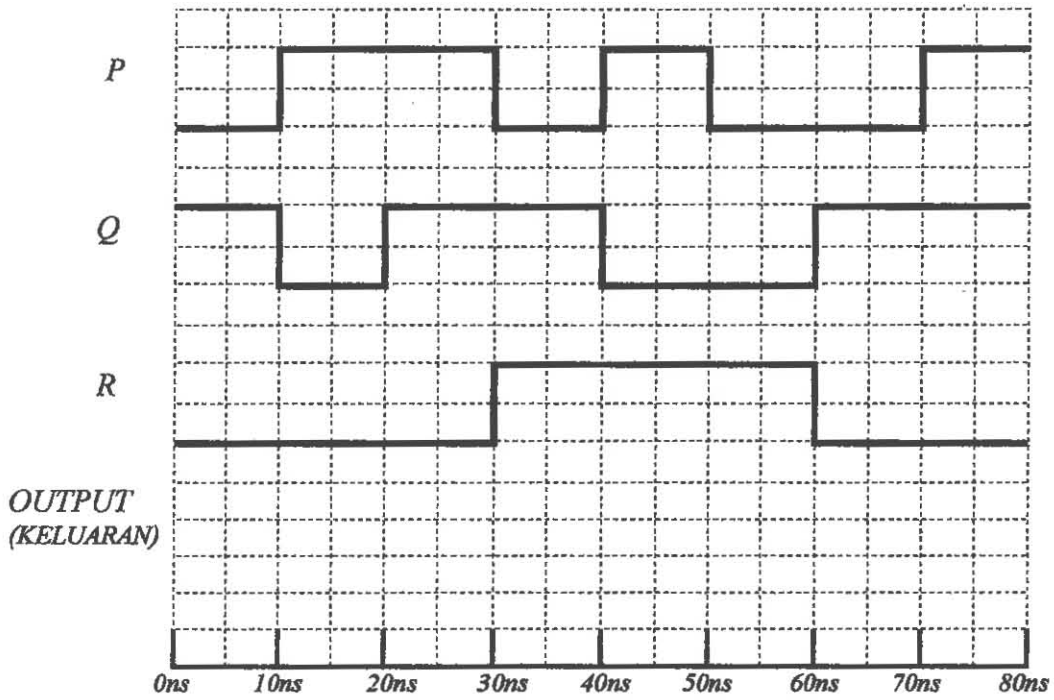
Appendix I
[Lampiran I]

Question 1(b)(iv)
[Soalan 1(b)(iv)]

Angka Giliran:_____ **No. Meja:** _____



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