UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Kedua
Sidang Akademik 2015/2016

Mac 2016

DMT241 – Introduction To Integrated Circuit Layout
[Pengenalan Kepada Pengantar Bentangan Litar Terkamir]

Masa: 3 jam

Please make sure that this question paper has **FOURTEEN (14)** printed pages including this front page before you start the examination.
*[Sila pastikan kertas soalan ini mengandungi **EMPAT BELAS (14)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This question paper has **SIX** questions. Answer **any FIVE** questions. Each question contributes 20 marks.
*[Kertas soalan ini mengandungi **ENAM** soalan. Jawab **mana-mana LIMA** soalan. Markah bagi tiap-tiap soalan adalah 20 markah.]*

Appendix I is given for **Question 1(c)(iv)**.
*[**Lampiran I** diberi untuk **Soalan 1(c)(iv)**.]*

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Question 1
[Soalan 1]

(a) First Integrated Circuit (IC) was invented by Jack Kilby from Texas Instruments in the year of 2000.
[Litar Bersepadu (IC) pertama telah direka oleh Jack Kilby dari Texas Instruments pada tahun 2000.]

(i) Define IC.
[Takrifkan IC.]

(2 Marks / *Markah*)

(ii) Name **TWO (2)** types of materials used to build transistor and the circuit inside an IC.
*[Namakan **DUA (2)** jenis bahan-bahan yang digunakan bagi membina transistor dan litar di dalam IC.]*

(1 Mark / *Markah*)

(iii) Explain **TWO (2)** applications of an IC.
*[Terangkan **DUA (2)** aplikasi-aplikasi sebuah IC.]*

(2 Marks / *Markah*)

(b) Most of modern IC's today used Complementary Metal Oxide Semiconductor (CMOS) technology as their basic technology.
[Kebanyakan IC moden hari ini menggunakan teknologi Pelengkap Separa Pengalir-Oksida-Logam (CMOS) sebagai teknologi asas mereka.]

(i) Name **TWO (2)** types of devices in CMOS.
[Namakan dua jenis peranti dalam CMOS.]

(1 Mark / *Markah*)

(ii) Define CMOS technology.
[Takrifkan teknologi CMOS.]

(3 Marks / *Markah*)

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(c) Refer to netlist in **Figure 1a.**
*[Rujuk netlist dalam **Rajah 1a.**]*

(i) Sketch the transistor level schematic.
[Lakarkan litar skematik aras transistor.]

(4 Marks / *Markah*)

(ii) Identify the Boolean equation.
[Kenalpasti persamaan Boolean.]

(1 Mark / *Markah*)

(iii) Write the testbench netlist using Piecewise Linear (PWL) source as the input signal in **Figure 1b** in **Appendix I.** Given VDD = 5V, GND = 0V, time delay (t_d) = rise time (t_r) = fall time (t_f) = 1ns.
*[Tuliskan "testbench netlist" menggunakan sumber Lelurus Cebisan (PWL) sebagai isyarat input di **Rajah 1b.** Diberikan VDD = 5V, GND = 0V, lengah masa (t_d) = masa naik (t_r) = masa jatuh (t_f) = 1ns.]*

(4 Marks / *Markah*)

(iv) Sketch the output waveform, OUT in **Appendix I.**
*[Lakarkan gelombang keluaran, OUT dalam **Lampiran I.**]*

(2 Marks / *Markah*)

```
.subckt QUESTION1  A     B     C     D     OUT

MP1   N1   A   VDD   VDD   p   L=0.4u   W=1u
MP2   OUT  B   N1    VDD   p   L=0.4u   W=1u
MP3   OUT  C   N1    VDD   p   L=0.4u   W=1u
MP4   OUT  D   N1    VDD   p   L=0.4u   W=1u
MN1   OUT  A   GND   GND   n   L=0.4u   W=1u
MN2   OUT  B   N2    GND   n   L=0.4u   W=1u
MN3   N2   C   N3    GND   n   L=0.4u   W=1u
MN4   N3   D   GND   GND   n   L=0.4u   W=1u

.ends QUESTION1
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Figure 1a
[Rajah 1a]

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Question 2
[Soalan 2]

(a) The chip complexity has increased by a factor of ~1000 since its first introduction.
[Kerumitan cip telah bertambah dengan satu faktor ~1000 sejak pengenalan pertamanya.]

(i) List **TWO (2)** industry trends of an Integrated Circuit (IC).
*[Senaraikan **DUA (2)** aliran industri sebuah Litar Bersepadu (IC).]*

(2 Marks / *Markah*)

(ii) Briefly explain the evolution of an IC in **Figure 2a.**
*[Terangkan secara ringkas evolusi IC dalam **Rajah 2a.**]*

(2 Marks / *Markah*)

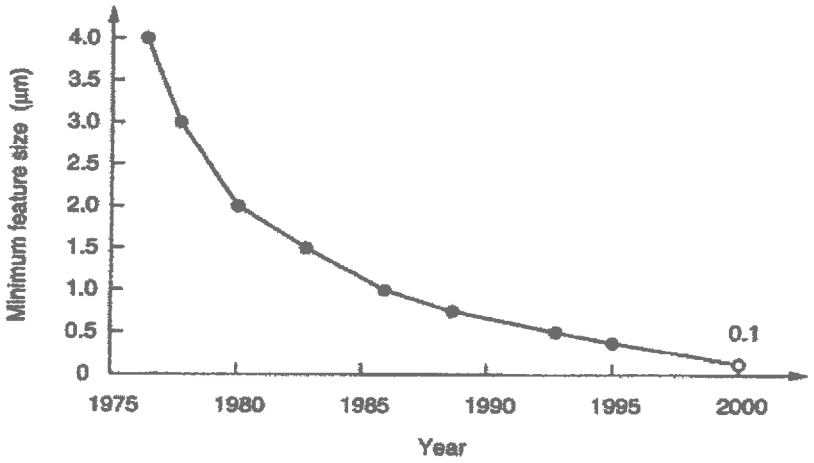

Figure 2a
[Rajah 2a]

(iii) List **FOUR (4)** classification of integration level of chip with its number of transistors.
*[Senaraikan **EMPAT (4)** pengkelasan tahap integrasi cip beserta dengan jumlah transistornya.]*

(2 Marks / *Markah*)

(b) Based on the equation below;
[Berdasarkan persamaan di bawah;]

$$Z = \overline{P + (\overline{QR})}$$

(i) simplified the equation by using De Morgan's Theorem.
[permudahkan persamaan tersebut dengan menggunakan Teorem De Morgan.]
(2 Marks / *Markah*)

(ii) state the number of transistors used in **(b)(i)**.
[nyatakan jumlah transistor yang digunakan dalam (b)(i).]
(1 Mark / *Markah*)

(iii) sketch the transistor level schematic in **(b)(ii)**.
[lakarkan litar skematik aras transistor dalam (b)(ii).]
(4 Marks / *Markah*)

(iv) write the netlist body for answer for **(b)(iii)**.
[tuliskan badan netlist untuk (b)(iii).]
(4 Marks / *Markah*)

(v) write a simulator netlist using PULSE source as in **Figure 2b**. Given $V_1 = 0V$, $V_2 = 5V$, time delay (t_d) = 0s, rise time (t_r) = fall time (t_f) = 1s.
*[tuliskan netlist pensimulasi menggunakan sumber PULSE seperti di **Rajah 2b**. Diberikan $V_1 = 0V$, $V_2 = 5V$, lengah masa (t_d) = 0s, masa naik (t_r) = masa jatuh (t_f) = 1s.]*
(3 Marks / *Markah*)

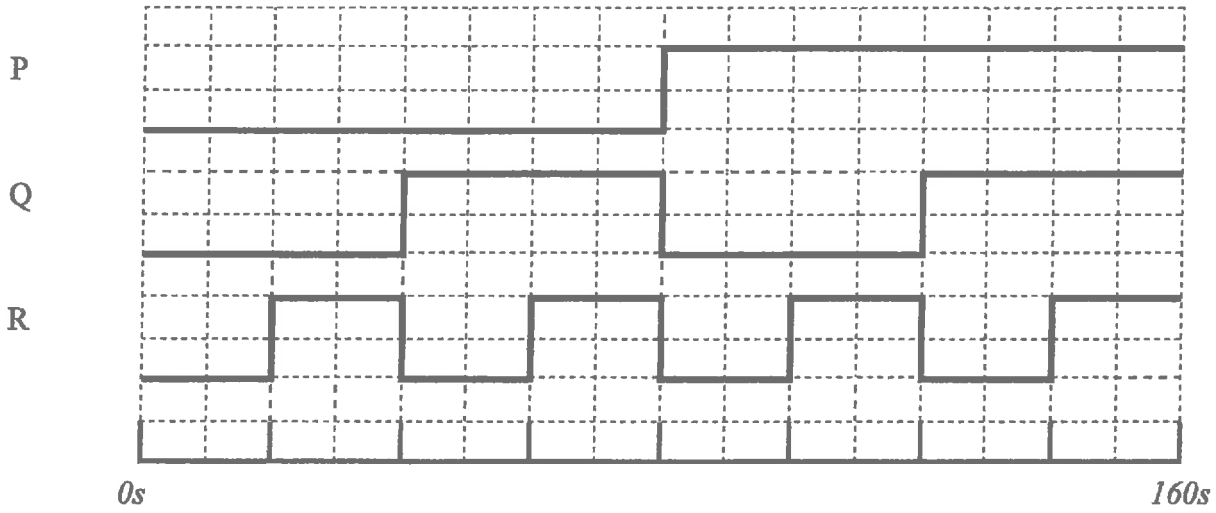

Figure 2b
[Rajah 2b]

Question 3
[Soalan 3]

(a) Differentiate NMOS and PMOS transistor in term of;
[Bezakan transistor NMOS dan PMOS berdasarkan terma;]

(i) structure.
[struktur.]

(2 Marks / *Markah*)

(ii) transistor as a switch.
[transistor sebagai suatu suis.]

(4 Marks / *Markah*)

(b) State **THREE (3)** operation regions for an NMOS transistor.
*[Nyatakan **TIGA (3)** keadaan operasi bagi sebuah transistor NMOS.]*

(3 Marks / *Markah*)

(c) With the aid of diagram, briefly explain answer in **(b)**.
*[Dengan bantuan gambarajah, terangkan secara ringkas jawapan di **(b)**.]*

(4 Marks / *Markah*)

(d) The NMOS transistor is designed with width/length = 8/2, t_{ox} = 100Å, μ_n = 350 cm^2/V.S and V_{TH} = 0.7V.
[Transistor NMOS direka bentuk dengan kelebaran/panjang = 8/2, t_{ox} = 100Å, μ_n = 350 cm^2/V.S.dan V_{TH} = 0.7V.]

(i) Calculate c_{ox} and β for the transistor.
[Kirakan c_{ox} dan β untuk transistor tersebut.]

(3 Marks / *Markah*)

(ii) Given the values of V_{GS} = 0.3V, 2.0V, 4.0V and 5V. Calculate the corresponding I_D values for each V_{GS} when the transistor is operating in the saturation region.
[Diberi nilai V_{GS} = 0.3V, 2.0V, 4.0V dan5V. Hitungkan nilai-nilai I_D sepadan untuk setiap V_{GS} apabila transistor beroperasi dalam keadaan tepu.]

(4 Marks / *Markah*)

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Question 4
[Soalan 4]

(a) Layout verification is done to ensure that the logic design and physical design will function correctly as expected.
[Pengesahan bentangan dibuat untuk memastikan bahawa reka bentuk logik dan reka bentuk fizikal akan berfungsi seperti yang dijangka.]

(i) Differentiate Design Rules Check (DRC) and Layout Versus Schematic (LVS).
[Bezakan Aturan Rekabentuk Memeriksa (DRC) dan Bentangan Lawan Skematik (LVS).]
(4 Marks / *Markah*)

(ii) With the aid of diagram, sketch an example for DRC and LVS error.
[Dengan bantuan gambarajah, lakar satu contoh untuk ralat DRC and LVS.]
(2 Marks / *Markah*)

(iii) Explain way to fix the error for answer in **(a)(ii)**.
[Jelaskan cara membetulkan ralat untuk jawapan di (a)(ii).]
(2 Marks / *Markah*)

(b) A Complementary Metal Oxide Semiconductor (CMOS) is a combinational of Pull Down Network (PDN) and Pull Up Network (PUN). Based on **Figure 4**;
*[Pelengkap Separa Pengalir-Oksida-Logam (CMOS) ialah satu kombinasi Rangkaian Tarik-Bawah (PDN) and Rangkaian Tarik-Naik (PUN). Berdasarkan **Rajah 4**;]*

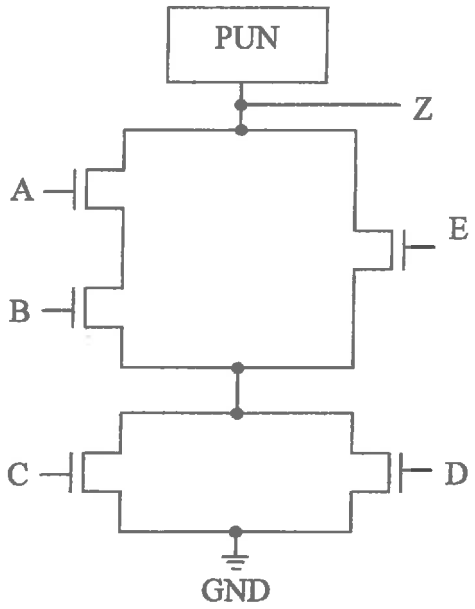

Figure 4
[Rajah 4]

(i) sketch the complete PUN for the schematic.
[lakarkan PUN lengkap untuk skematik tersebut.]

(5 Marks / *Markah*)

(ii) identify the Boolean equation for the output, Z.
[kenalpasti persamaan Boolean untuk keluaran, Z.]

(1 Mark / *Markah*)

(iii) sketch the Eular path for {B, A, E, D, C}.
[lakarkan laluan Eular bagi {B, A, E, D, C}.]

(1 Mark / *Markah*)

(iv) sketch the stick diagram for the schematic.
[lakarkan gambarajah ranting bagi skematik tersebut.]

(5 Marks / *Markah*)

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Question 5
[Soalan 5]

(a) Bipolar Junction Transistor (BJT) is an active semiconductor device formed by two p-n junctions.
[Persimpangan Dwikutub Transistor (BJT) ialah sebuah peranti semikonduktor aktif dibentuk oleh dua simpang p-n.]

(i) With the aid of diagram, give **TWO (2)** configurations for this device.
[Dengan bantuan gambarajah, berikan DUA (2) konfigurasi-konfigurasi bagi peranti ini.]
(2 Marks / *Markah*)

(ii) Name the mechanism of particle diffusion for answer in **(a)(i)**.
[Namakan mekanisme resapan zarah untuk jawapan di (a)(i).]
(1 Mark / *Markah*)

(iii) **Figure 5(a)** shows the operating region for an NPN transistor. State the operating region for the circled number.
***[Rajah 5(a)** menunjukkan kawasan operasi untuk satu transistor NPN. Nyatakan kawasan operasi bagi nombor yang dibulatkan.]*
(1 Mark / *Markah*)

(iv) Briefly explain saturation region.
[Terangkan dengan ringkas kawasan ketepuan.]
(2 Marks / *Markah*)

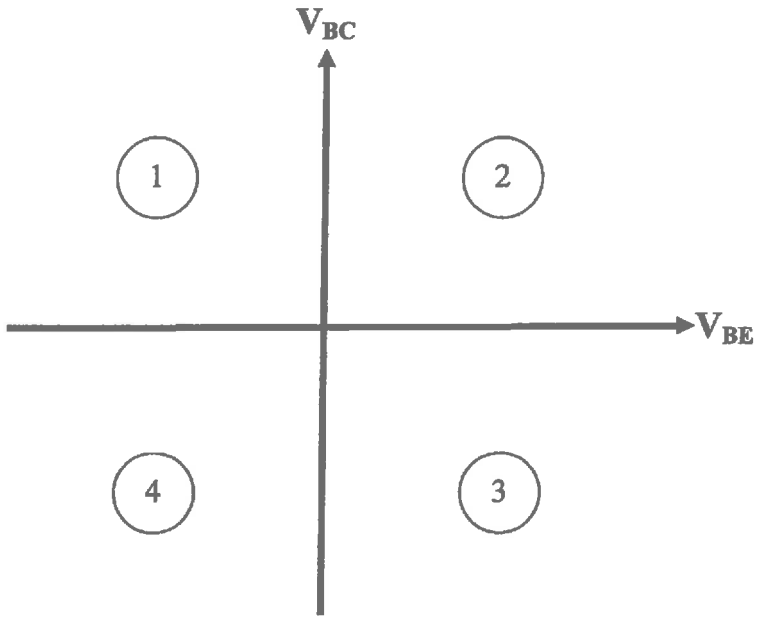
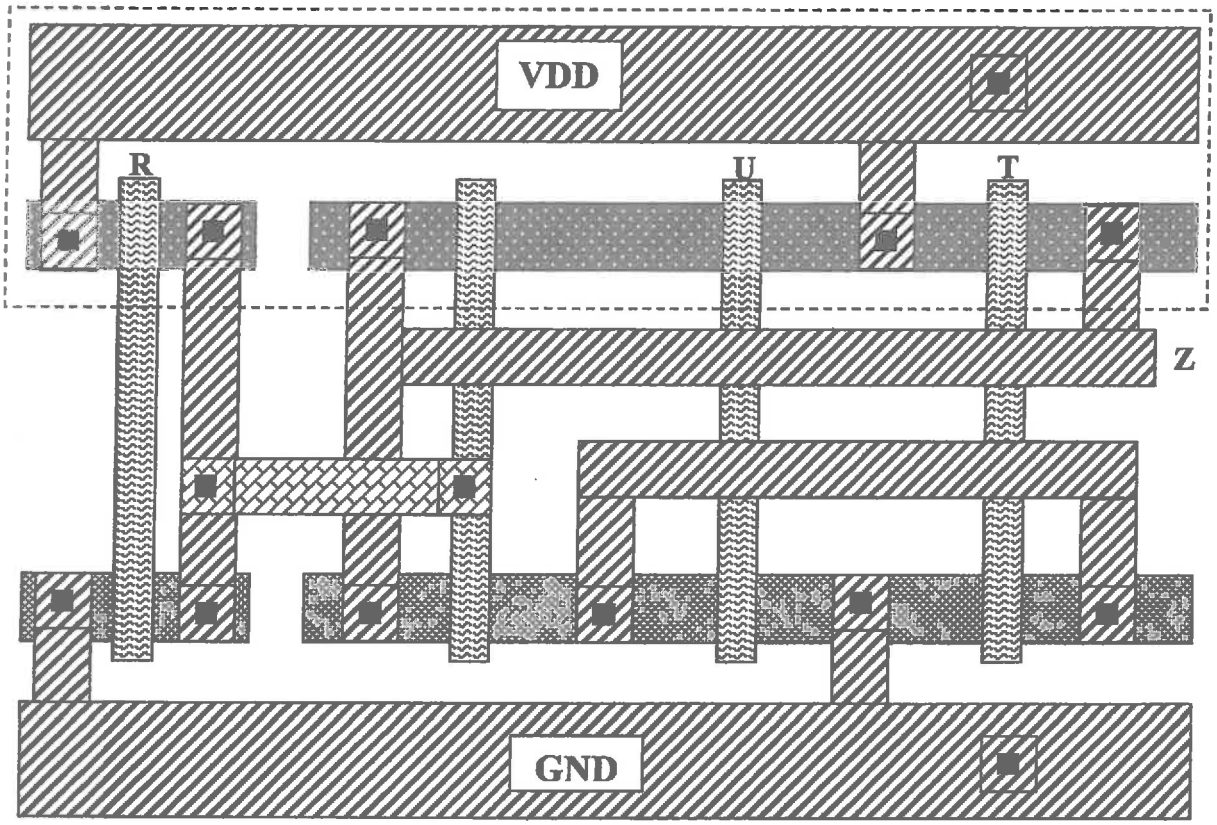


Figure 5(a)
[Rajah 5(a)]

(b) Based on **Figure 5(b)**:
*[Berdasarkan **Rajah 5(b)**:]*



Legend:
[Petunjuk:]

P-diffusion
N-diffusion
Polysilicon
N-well
Contact
Metal 1
Metal 2

Figure 5(b)
[Rajah 5(b)]

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(i) sketch the stick diagram.
[lakarkan gambarajah ranting.]

(2 Marks / *Markah*)

(ii) sketch the corresponding transistor level schematic.
[lakarkan skematik aras transistor yang sepadan.]

(7 Marks / *Markah*)

(iii) derive the Boolean equation for the schematic.
[terbitkan persamaan Boolean bagi skematik tersebut.]

(1 Mark / *Markah*)

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Question 6
[Soalan 6]

(a) An Application Specific Integrated Circuits (ASICs) is an integrated circuit customized for particular used in an IC. Explain **TWO (2)** advantages of ASICs.
*[Litar Terkamil Beraplikasi Spesifik (ASICs) ialah satu litar bersepadu dibuat megikut perincian pesanan untuk digunakan dalam satu IC. Jelaskan **DUA (2)** kelebihan-kelebihan ASICs.]*

(2 Marks / *Markah*)

(b) Dynamic and static logic are two types of CMOS families. Differentiate dynamic and static logic.
[Logik dinamik dan statik ialah dua jenis keluarga-keluarga CMOS. Bezakan logik dinamik dan statik.]
(4 Marks / *Markah*)

(c) Refer to **Figure 6**;
*[Rujuk **Rajah 6**;]*

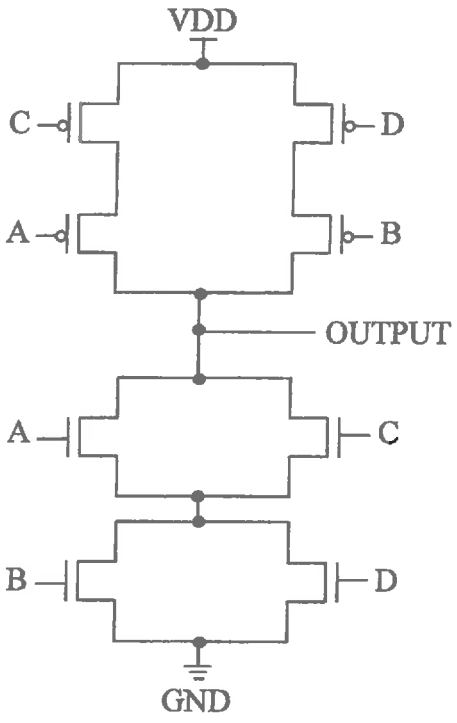

Figure 6
[Rajah 6]

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(i) sketch the Eular path for the schematic.
[lakarkan laluan Eular bagi skematik tersebut.]

(1 Mark / *Markah*)

(ii) sketch the stick diagram based on answer in **(c)(i)**.
[lakarkan gambarajah ranting bagi jawapan di (c)(i).]

(4 Marks / *Markah*)

(iii) draw the layout for **(c)(ii)** based on TSMC 0.35μm technology by using graph paper. Given length, $L = 2\lambda$ and width, $W = 5\lambda$ for the transistors. Label the width and spacing. (Use ratio 1λ : 2mm).
[lukiskan bentangan untuk (c)(ii) berdasarkan teknologi TSMC 0.35μm dengan menggunakan kertas graf. Diberi panjang, $L = 2\lambda$ dan lebar, $W = 5\lambda$ bagi transistor-transistor tersebut. Labelkan lebar dan jarak. (Gunakan nisbah 1λ : 2mm).]

(9 Marks / *Markah*)

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Appendix I
[Lampiran I]

Question 1(c) (iv)
[Soalan 1(c) (iv)]

Angka Giliran:_____ **No. Meja:** _____

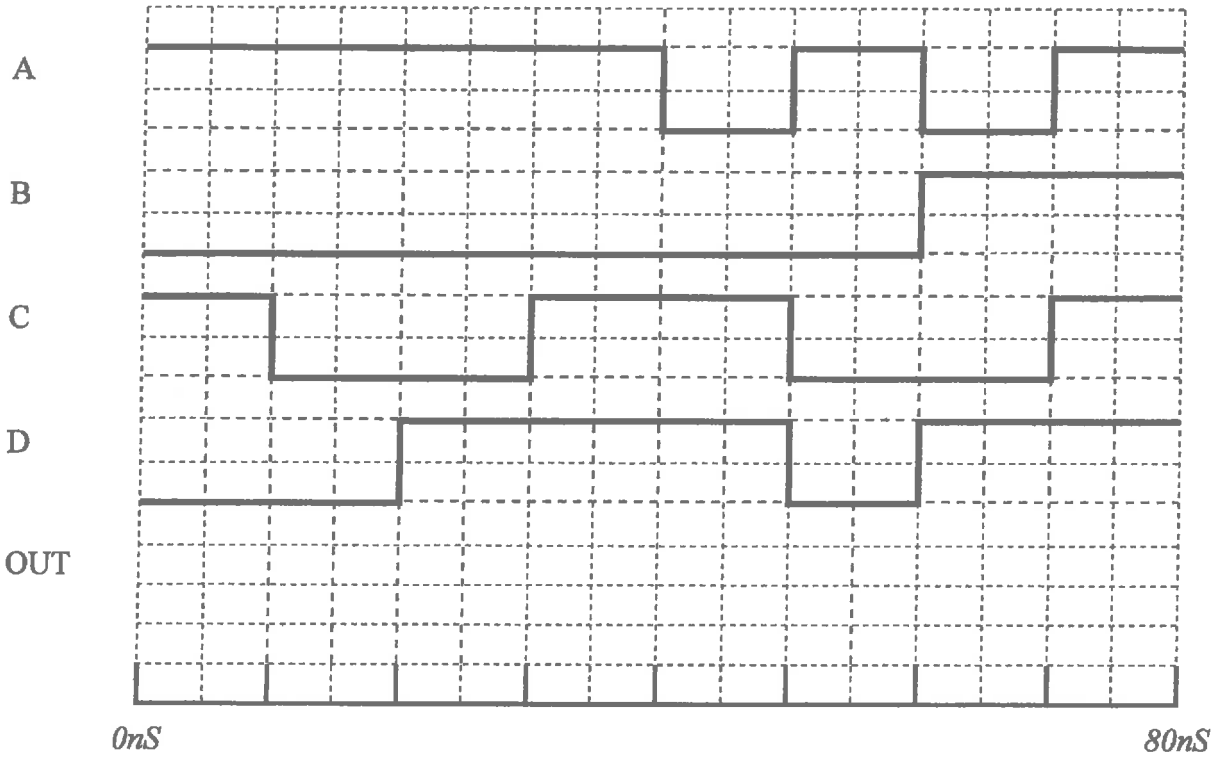

Figure 1b
[Rajah 1b]