UNIVERSITI MALAYSIA PERLIS

Peperiksaan Semester Kedua
Sidang Akademik 2016/2017

Mac 2017

DMT241 – Introduction To Integrated Circuit Layout
[Pengenalan Kepada Pengantar Bentangan Litar Terkamir]

Masa: 3 jam

Please make sure that this question paper has **FIFTEEN (15)** printed pages including this front page before you start the examination.
*[Sila pastikan kertas soalan ini mengandungi **LIMA BELAS (15)** muka surat yang bercetak termasuk muka hadapan sebelum anda memulakan peperiksaan ini.]*

This paper contains **PART A** and **PART B**. Answer **ALL** questions in **PART A** and choose any **ONE** question in **PART B**. Each question contributes 20 marks.
*[Kertas ini mengandungi **BAHAGIAN A** and **BAHAGIAN B**. Jawab **SEMUA** soalan dalam **BAHAGIAN A** dan pilih mana-mana **SATU** soalan dalam **BAHAGIAN B**. Markah bagi tiap-tiap soalan adalah 20 markah.]*

Please answer questions 1(d)(iv), 2(c)(iv) and 4(a)(iv) in **Appendix I, II** and **III** respectively.
*[Sila jawab soalan-soalan 1(d)(iv), 2(c)(iv) dan 4(a)(iv) masing-masing dalam **Lampiran I, II dan III**.]*

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PART A
[BAHAGIAN A]

Question 1
[Soalan 1]

(a) List **THREE (3)** advantages of constructing circuit in Integrated Circuit (IC) compared to discrete components.
*[Senaraikan **TIGA (3)** kelebihan-kelebihan pembinaan litar dalam Litar Terkamir (IC) berbanding komponen-komponen diskret.]*

(3 Marks/ *Markah*)

(b) Sketch and define Moore's Law.
[Lakar dan takrifkan Hukum Moore.]

(3 Marks/ *Markah*)

(c) With the aid of diagram, explain the operation region of a NMOS transistor.
[Dengan bantuan gambarajah, jelaskan kawasan operasi bagi sebuah transistor NMOS.]

(3 Marks/ *Markah*)

(d) Refer to netlist in **Figure 1(a)**.
*[Rujuk netlist dalam **Rajah 1(a)**.]*

```
.subckt QUESTION1 A B C Y

    MN4    N1    A    GND   GND   n   L=2u  W=5u
    MN3    Y     N2   N1    GND   n   L=2u  W=5u
    MN2    Y     B    N1    GND   n   L=2u  W=5u
    MN1    N2    C    GND   GND   n   L=2u  W=5u
    MP4    N2    C    VDD   VDD   p   L=2u  W=5u
    MP3    Y     A    VDD   VDD   p   L=2u  W=5u
    MP2    Y     N2   N3    VDD   p   L=2u  W=5u
    MP1    N3    B    VDD   VDD   p   L=2u  W=5u

.ends QUESTION1
```

Figure 1(a)
[Rajah 1(a)]

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(i) Sketch the transistor level schematic.
[Lakarkan litar skematik aras transistor.]

(4 Marks/ *Markah*)

(ii) Identify the Boolean equation.
[Kenalpasti persamaan Boolean.]

(1 Mark/ *Markah*)

(iii) By referring **Figure 1(b)** in **Appendix I**, produce the testbench netlist using Piecewise Linear (PWL) source as the input signal. Given VDD = 5V, GND = 0V, time delay (t_d) = rise time (t_r) = fall time (t_f) = 1ns.
*[Dengan merujuk **Rajah 1(b)** dalam **Lampiran I**, hasilkan "testbench netlist" menggunakan sumber Lelurus Cebisan (PWL) sebagai isyarat input. Diberikan VDD = 5V, GND = 0V, lengah masa (t_d) = masa naik (t_r) = masa jatuh (t_f) = 1ns.]*

(4 Marks/ *Markah*)

(iv) Sketch the output waveform, Y in **Appendix I**.
*[Lakarkan gelombang keluaran, Y dalam **Lampiran I**.]*

(2 Marks/ *Markah*)

Question 2
[Soalan 2]

(a) Briefly explain;
[Terangkan dengan ringkas;]

(i) transient analysis.
[analisa transien.]

(2 Marks/ *Markah*)

(ii) .lib term.
[istilah .lib.]

(2 Marks/ *Markah*)

(b) Explain the operation of Complementary Metal Oxide Semiconductor (CMOS) inverter.
[Jelaskan operasi penyongsang Separa Pengalir-Oksida-Logam (CMOS).]

(2 Marks/ *Markah*)

(c) Based on the equation below;
[Berdasarkan persamaan di bawah;]

$$F = Y + XZ$$

(i) sketch the transistor level schematic.
[lakarkan litar skematik aras transistor.]

(4 Marks/ *Markah*)

(ii) produce the netlist body for answer in(c)(i).
[hasilkan badan netlist dalam (c)(i).]

(5 Marks/ *Markah*)

(iii) By referring **Figure 2** in **Appendix II**, produce a simulator netlist using PULSE source. Given V_1 = 0V, V_2 = 5V, time delay (t_d) = 0s, rise time (t_r) = fall time (t_f) = 1s.
*[Dengan merujuk **Rajah 2** dalam **Lampiran II**, hasilkan netlist pensimulasi menggunakan sumber PULSE. Diberikan V_1 = 0V, V_2 = 5V, lengah masa (t_d) = 0s, masa naik (t_r) = masa jatuh (t_f) = 1s.]*

(3 Marks/ *Markah*)

(iv) sketch the output waveform, F in **Appendix II**.
*[lakarkan gelombang keluaran, F dalam **Lampiran II**.]*

(2 Marks/ *Markah*)

Question 3
[Soalan 3]

(a) Bipolar Junction Transistor (BJT) is a semiconductor device constructed with three doped semiconductor regions (base, collector and emitter) separated by two p-n junctions.
[Persimpangan Dwikutub Transistor (BJT) ialah satu peranti semikonduktor dibina dengan tiga buah rantau separuh pengalir terdop (asas, pengumpul dan pemancar) dipisahkan oleh dua simpang p-n.]

(i) List **TWO (2)** types of BJT.
[Senaraikan DUA (2) jenis BJT.]

(2 Marks/ *Markah*)

(ii) Sketch the symbol for answer in **(a)(i)**.
[Lakarkan symbol bagi jawapan dalam (a)(i).]

(2 Marks/ *Markah*)

(iii) Name the circled number in **Figure 3**.
*[Namakan nombor yang dibulatkan dalam **Rajah 3**.]*

(1 Mark/ *Markah*)

(iv) Explain answer in **(a)(iii)**.
[Terangkan jawapan dalam (a)(iii).]

(4 Marks/ *Markah*)

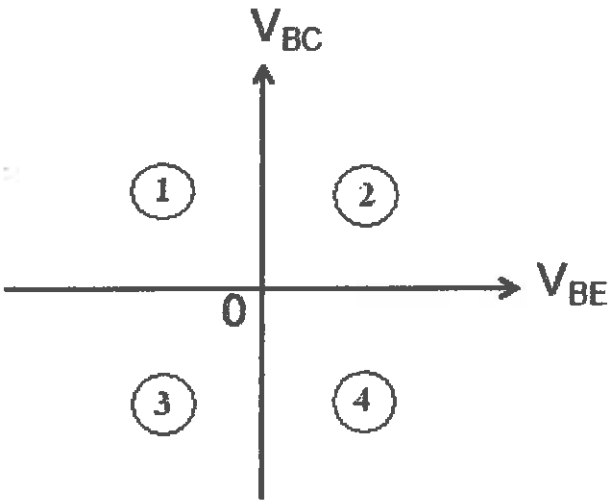

Figure 3
[Rajah 3]

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(b) The NMOS transistor is designed with width/length = 10/4, t_{ox} = 150Å, μ_n = 350 cm^2/V.S and V_{TH} = 0.7V.
[Transistor NMOS direka bentuk dengan kelebaran/panjang = 10/4, t_{ox} = 150Å, μ_n = 350 cm^2/V.S.dan V_{TH} = 0.7V.]

(i) Calculate c_{ox} and β for the transistor.
[Kirakan c_{ox} dan β untuk transistor tersebut.]

(3 Marks/ *Markah*)

(ii) Given the values of V_{GS} = 0.3V, 2.0V, 4.0V and 5V. Calculate the corresponding I_D values for each V_{GS} when the transistor is operating in the saturation region.
[Diberi nilai V_{GS} = 0.3V, 2.0V, 4.0V dan5V. Kirakan nilai-nilai I_D sepadan untuk setiap V_{GS} apabila transistor beroperasi dalam keadaan tepu.]

(4 Marks/ *Markah*)

(iii) Sketch graph I_D versus V_{DS} for answer in **(b)(ii)**.
[Lakarkan graf I_D melawan V_{DS} bagi jawapan dalam (b)(ii).]

(4 Marks/ *Markah*)

Question 4
[Soalan 4]

(a) Based on **Figure 4(a);**
*[Berdasarkan kepada **Rajah 4(a);**]*

(i) express the Boolean equation for the circuit.
[nyatakan persamaan Boolean bagi litar tersebut.]

(2 Marks/ *Markah*)

(ii) simplified the Boolean equation by using De Morgan's theorem.
[permudahkan persamaan Boolean dengan menggunakan teorem De Morgan.]

(2 Marks/ *Markah*)

(iii) sketch the corresponding transistor level schematic in **(a)(ii).**
[lakarkan skematik aras transistor yang sepadan dalam (a)(ii).]

(4 Marks/ *Markah*)

(iv) predict the output, OUT waveform in **Appendix III.**
*[ramalkan gelombang keluaran, OUT dalam **Lampiran III.**]*

(2 Marks/ *Markah*)

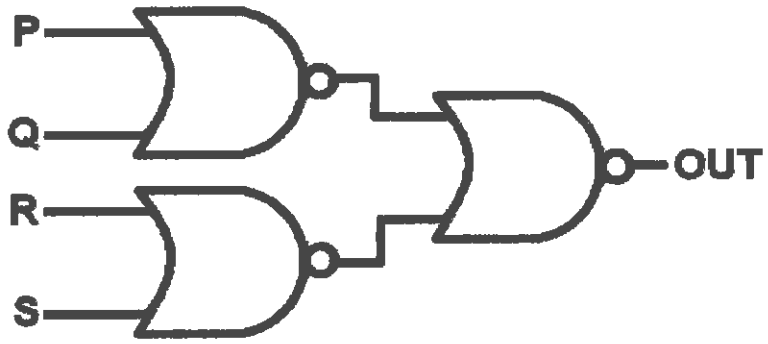

Figure 4(a)
[Rajah 4(a)]

(b) A Complementary Metal Oxide Semiconductor (CMOS) is a combinational of Pull Down Network (PDN) and Pull Up Network (PUN). Based on **Figure 4(b)**;
*[Pelengkap Separa Pengalir-Oksida-Logam (CMOS) ialah satu kombinasi Rangkaian Tarik-Bawah (PDN) and Rangkaian Tarik-Naik (PUN). Berdasarkan **Rajah 4 (b)**;]*

(i) sketch the appropriate PDN for the schematic.
[lakarkan PDN yang sesuai untuk skematik tersebut.]
(4 Marks/ *Markah*)

(ii) express the Boolean equation for the output, Z.
[nyatakan persamaan Boolean untuk keluaran, Z.]
(1 Mark/ *Markah*)

(iii) sketch the stick diagram for the schematic using Eular path {D, B, A, C}.
[lakarkan gambarajah ranting bagi skematik tersebut menggunakan laluan Eular {D, B, A, C}.]
(5 Marks/ *Markah*)

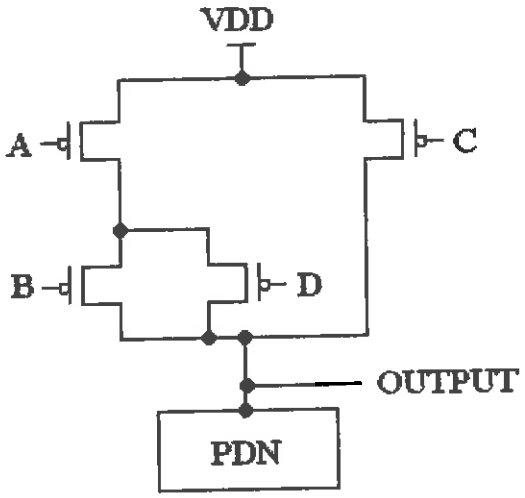

Figure 4(b)
[Rajah 4(b)]

PART B
[BAHAGIAN B]

Question 5
[Soalan 5]

(a) Differentiate poly-contact and via in an IC design.
[Bezakan sentuhan-poly dan "via" dalam rekabentuk sebuah IC.]

(2 Mark/ *Markah*)

(b) The generated layout must pass a series of checks in a process known as layout verification.
[Bentangan yang dijana mesti lulus satu siri semakan-semakan dalam satu proses dikenali sebagai pengesahan bentangan.]

(i) List **ONE (1)** of the layout verification.
*[Senaraikan **SATU (1)** daripada pengesahan bentangan.]*

(1 Mark/ *Markah*)

(ii) Give **ONE (1)** error according to the answer in **(b)(i)**.
*[Berikan **SATU (1)** contoh bagi jawapan dalam **(b)(i)**.]*

(1 Mark/ *Markah*)

(iii) Explain way to solve the error as answer in **(b)(ii)**.
*[Jelaskan jalan penyelesaian bagi ralat seperti jawapan dalam **(b)(ii)**.]*

(2 Marks/ *Markah*)

(c) **Figure 5** shows the stick diagram for a CMOS combinational logic gate. Based on the figure;
***[Rajah 5** menunjukkan gambarajah ranting bagi sebuah gabungan get logic CMOS. Berdasarkan gambarajah tersebut;]*

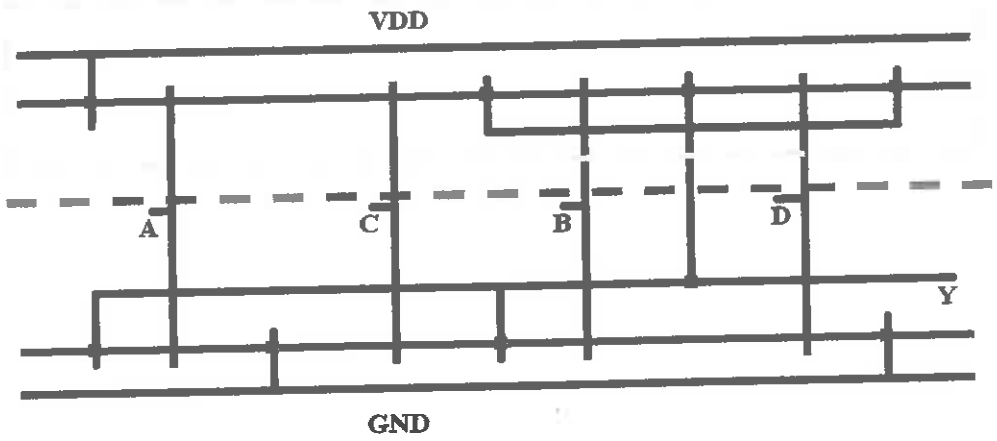

Figure 5
[Rajah 5]

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(i) sketch the corresponding transistor level schematic.
[lakarkan skematik aras transistor yang sepadan.]

(4 Marks/ *Markah*)

(ii) express the Boolean expression for output, Y.
[nyatakan persamaan Boolean bagi keluaran, Y.]

(1 Mark/ *Markah*)

(iii) sketch the gate level schematic for answer in **(c)(ii)**.
[lakarkan schematic aras get bagi jawapan dalam (c)(ii).]

(2 Marks/ *Markah*)

(iv) construct the layout for **(c)(iii)** based on TSMC 0.35µm technology by using graph paper. Given length, L = 2λ and width, W = 5λ for the transistors. Label at least **FOUR (4)** design rules must be followed. (Use ratio 1λ : 2mm).
[binakan bentangan untuk (c)(iii) berdasarkan teknologi TSMC 0.35µm dengan menggunakan kertas graf. Diberi panjang, L = 2λ dan lebar, W = 5λ bagi transistor-transistor tersebut. Labelkan sekurang-kurangnya EMPAT (4) aturan rekabentuk yang mesti dipatuhi. (Gunakan nisbah 1λ : 2mm).]

(7 Marks/ *Markah*)

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Question 6
[Soalan 6]

(a) List and differentiate **TWO (2)** types of CMOS families.
[Senarai dan bezakan DUA (2) jenis keluarga CMOS.]

(3 Marks/ *Markah*)

(b) Illustrate and explain the connection of active to metal-2 layer.
[Lakar dan terangkan sambungan lapisan aktif ke lapisan logam-2.]

(3 Marks/ *Markah*)

(c) Refer to **Figure 6;**
*[Rujuk **Rajah 6;**]*

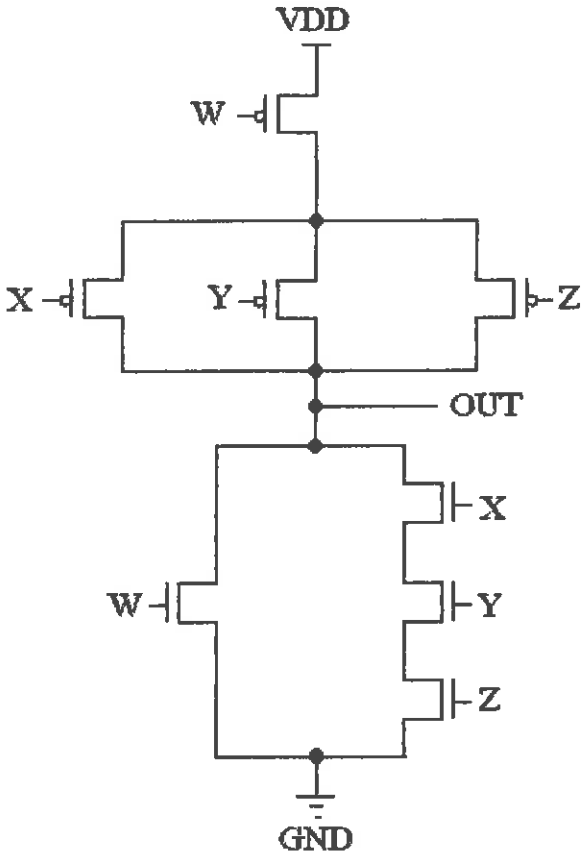

Figure 6
[Rajah 6]

(i) identify the Boolean equation.
[kenalpastikan persamaan Boolean.]

(1 Mark/ *Markah*)

(ii) sketch and give the Eular path for the schematic.
[lakar dan berikan laluan Eular bagi skematik tersebut.]

(1 Mark/ *Markah*)

(iii) sketch the stick diagram based on answer in **(c) (ii)**.
[lakarkan gambarajah ranting bagi jawapan di (c)(ii).]

(4 Marks/ *Markah*)

(iv) construct the layout for **(c)(iii)** based on TSMC 0.35µm technology by using graph paper. Given length, L = 2λ and width, W = 5λ for the transistors. Label at least **FOUR (4)** design rules must be followed. (Use ratio 1λ : 2mm).
[binakan bentangan untuk (c)(iii) berdasarkan teknologi TSMC 0.35µm dengan menggunakan kertas graf. Diberi panjang, L = 2λ dan lebar, W = 5λ bagi transistor-transistor tersebut. Labelkan sekurang-kurangnya EMPAT (4) aturan rekabentuk yang mesti dipatuhi. (Gunakan nisbah 1λ : 2mm).]

(8 Marks/ *Markah*)

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Appendix I
[Lampiran I]

Question 1(d)(iv)
[Soalan 1(d)(iv)]

Angka Giliran:_____ **No. Meja:** _____

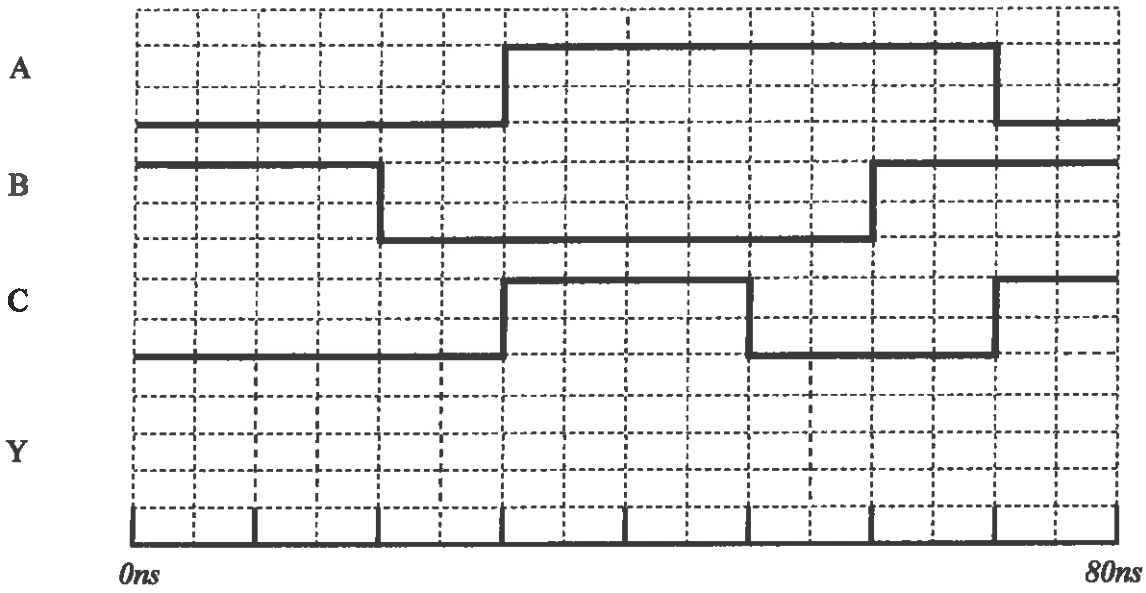

Figure 1(b)
[Rajah 1(b)]

Appendix II
[Lampiran II]

Question 2(c)(iv)
[Soalan 2(c)(iv)]

Angka Giliran:_____ **No. Meja:** _____

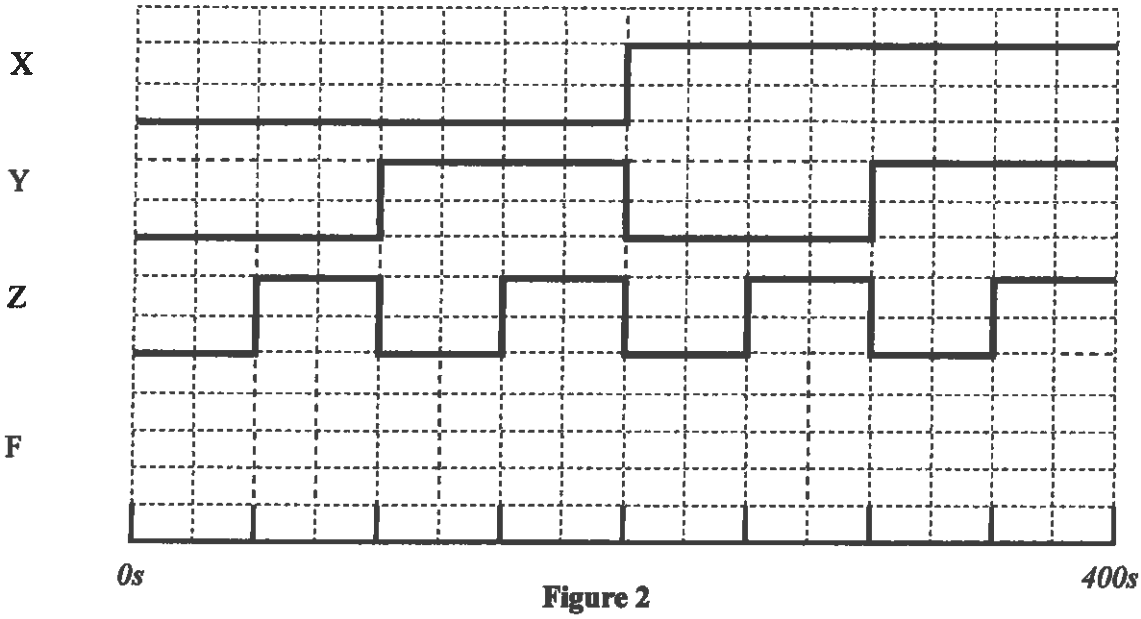

Figure 2
[Rajah 2]

Appendix III
[Lampiran III]

Question 4(a)(iv)
[Soalan 4(a)(iv)]

Angka Giliran:_____ **No. Meja:** _____